Design of CMOS Current-Mode Analog Computational Circuits

BY

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Dedication

To

my great mother,

my noble father ,

my lovely wife,

my warmhearted brothers and sisters,

my son Saleh,

and my dear uncle Awadh

your love is the source of my strength

ACKNOWLEDGMENTS

First and foremost all praise to Almighty Allah who gave me the faith and ability to complete this work successfully.

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GLOSSARY

Symbol	Quantity	Unit
V_{th}	Threshold voltage	V
λ	Channel length modulation factor	1/V
V_{DSP}	Drain-to-source pinch-off voltage	V
V_{GS}	Gate-to-source voltage	V
V_{eff}	Effective gate-source voltage	V
I_{Do}	Leakage current	A
n	Weak inversion slope factor	–
V_{BS}	Body-source voltage	V
V_T	Thermal voltage (≈25mV at room temperature)	V
K	Boltzmann constant $(1.38 * 10^{-23})$	$J/{}^{\circ}K$
T	Absolute temperature	K
q	Charge of an electron $(1.6 * 10^{-19})$	C
k'_n	Process transconductance parameter	$\frac{A}{V^2}$
μ_n	The mobility of charge carriers	$\frac{cm^2}{V.s}$
C_{ox}	Normalized oxide capacitance (capacitor per unit gate area)	$\frac{F}{m^2}$
ϵ_{ox}	Permittivity of the silicone oxide	$\frac{F}{m}$
t_{ox}	Thickness of the oxide layer	m
W	Channel width	m
L	Channel length	m
SNR	Signal-to-Noise Ratio	dB
V_{DD}	Positive supply voltage	V
V_{SS}	Negative supply voltage	V
V_{th0}	Threshold voltage at V_{BS}=0	V
γ	Bulk-threshold parameter typical value of $0.7V^{-\frac{1}{2}}$	$V^{-\frac{1}{2}}$
$\emptyset_b$	Surface-potential (typical value of 0.6V)	V

V_{DS}	Drain-to-source voltage	V
I_{DS}	Drain-to-source current	A

ABSTRACT

Full Name : Karama Mohammed Karama AL-Tamimi

Thesis Title : Design of Low Voltage Low Power Current Mode Analog Computational Unit Using MOSFETs in Weak Inversion

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The major objective of this research is to design low-voltage current-mode logarithmic and exponential circuits using MOSFETs in weak inversion region. In this regard, two different structures for current-input current-output logarithmic amplifiers and 96dB linear exponential function generator are proposed. The proposed circuits are simulated with standard CMOS 0.35µm process technology to validate the theoretical analysis. Simulation results confirm that the proposed structures achieve the required goals in terms of low voltage operation and low power consumption while at the same time show stable performance with temperature and process variations. To demonstrate the effectiveness, logarithmic and exponential circuits are used as core cells to introduce different analog signal processing applications such as computational circuit and variable gain amplifiers (VGAs).

ملخص الرسالة

الإسم الكامل : كرامه بن محمد كرامه التميمي

عنوان الرسالة : تصميم ومحاكاة معالج إشارات تماثلية قليل الإستهلاك للجهد والطاقة بإستخدام ترانزستورات MOSFET تعمل في منطقة تحت جهد العتبة

التخصص : الهندسة الكهربائية

تاريخ الدرجة العلمية : ديسمبر 2012

الهدف الرئيسي من هذا البحث هو تصميم دوائر المكبّر اللوغاريتمي والدالة الأسية قليلة الأستهلاك للجهد والطاقة بإستخدام ترانزستورات MOSFETs في منطقة الإنقلاب الضعيف (تحت جهد العتبة). في هذا الصدد، تم تصميم دائرتين مختلفة للمكبّر اللوغاريتمي بنمط التيار بالإضافة إلى دائرة دالّة أسيّة لها نطاق خرج خطي واسع يصل إلى 96dB. تم محاكاة الدوائر المقترحة بواسطة تكنولوجيا CMOS 0.35µm للتحقق من صحة التحليل النظري. نتائج المحاكاة تؤكد أن الدوائر المقترحة تحقق الأهداف المطلوبة من حيث الإستهلاك القليل للجهد والطاقة، وفي ذات الوقت تظهر أداء مستقر مع تغيّر درجة الحرارة أو عدم التوافق في النبائط. وللتدليل على فعاليّة الدوائر اللوغاريتمية والأسيّة، تم إستخدامها في تصميم أنظمة مختلفة لتطبيقات معالجة الإشارات التناظرية مثل دائرة العمليات الحسابية والمكبرات ذات الكسب المتغيّر (VGAs).

CHAPTER 1

INTRODUCTION

1.1 Motivation

With the rapid advance in technology and applications, ultra low power systems are required in many applications such as portable or mobile battery powered devices, systems that function by harvesting power from environment, systems where heat dissipation should be minimized, complex systems and systems where the overall cost is function of the size of the system. Many techniques have been proposed to develop circuits that dissipate low power. One of these techniques is design circuits using MOSFETs in subthreshold that allow generating current in the range of nano-ampers.

The need to carry out signal processing on the signals in its analog form will assure faster and lower design cost. Moreover, with the development of new technologies and the advent of portable battery powered systems; for example wireless sensors networks, biomedical circuits, cell phones, there is an increasing interest in energy-aware circuit design techniques.

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amounts of energy. While performance and area remain to be two major design goals, power consumption has become a critical concern in today’s VLSI system design [1]. The need for low-power VLSI systems arises from two main forces. First, with the steady growth of processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices.

Also, with shrinking technology sizes, energy efficiency has become a critical aspect of designing digital circuits. Traditionally, voltage scaling, a mechanism in which the supply voltage is varying and the threshold voltage is constant, has been an effective solution in meeting stringent energy requirements. However, voltage scaling does come at a cost of reduction in performance. The limits of voltage scaling, and therefore energy minimization, can be explored by operating a circuit at subthreshold [2]. In subthreshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor. Due to the significant reduction in power with respect to the supply voltage, subthreshold circuits are classified as *ultra low power circuits*. Specifically in application areas where speed can be sacrificed for low power, subthreshold circuits are ideal fit e.g. medical applications and battery operated devices such as cellular phones.

Also, there is increasing demand for more logic functionality: that is, an IC must be capable of performing more functions, particularly as a combined set of designs on a single chip.

Today's designers have to make some important decisions among the conflicting limits on IC operation that are imposed by performance demands and reliability constraints. Examination of the key issues involved in MOSFET design for high-performance ICs can help guide designers out of this dilemma. These issues include the operating limits imposed by the differing requirements of speed, reliability, and power dissipation. In addition, conflicts involving process complexity and manufacturing cost go beyond the trade-offs that apply to operation. We can link the emerging trend of decreasing the supply voltage (V_{DD}) to this second trade-off, as supply voltage reduction enables active power reduction with increased performance. While the supply voltage can be reduced, constraints due to increasing numbers of transistors per IC, combined with more aggressive passive power requirements, make it impossible to further reduce the designed MOSFET threshold voltage [3].

1.2 Why Low Power Designs

Even when power is available in nonportable applications, the issue of low power design is becoming critical. Up until now, this power consumption has not been of great concern, since large packages and other cooling techniques have been capable of dissipating the generated heat. However, as the density and size of the chips and systems continue to increase, the difficulty in providing adequate cooling might either add significant cost to the system or provide a limit on the amount of functionality that can be provided [4].

While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size of the integrated circuits. If this exponential rise in the power density were to increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electromigration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance. Thus, it is evident that the methodologies for the design of low power digital systems are needed.

Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. For battery-portable systems running on batteries such as, laptops, cellular phones and personal digital assistants (PDAs), low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field. Hence, motivated by emerging battery operated applications that demand intensive computation in portable environments such as pacemakers and cellular phones etc, techniques are investigated which reduce power consumption in CMOS circuits, by operating the devices at low currents and low voltages. It is known that MOSFET devices and circuits especially CMOS circuits consume relatively low power. But there seems to be a need to reduce this power further to prolong the life of battery [5].

1.3 Why Analog Design

The world around us is analog, and the need to carry out signal processing on the signals in its analog form will assure faster and lower cost designs. Moreover, with the development of new technologies and the advent of portable battery powered systems; for example wireless sensors networks, biomedical circuits, cell phones, there is an increasing interest in energy-aware circuit design techniques.

Low voltage and low power design techniques are, therefore, attracting the interest of both manufacturers and users. Subthreshold operation of MOSFETs, in which the power supply voltage is lowered to below the transistor threshold voltage, enables drastic savings when energy rather than speed is the primary constraint. Operating the MOSFET in subthreshold region is, therefore, a possible approach to achieve low voltage and low power design.

While CMOS circuits operating in the subthreshold region have been inadequate for high speed applications, they have been used in applications that require ultra low power dissipation. With technology scaling, power supply and threshold voltage continue to decrease to satisfy high performance and low power requirements. This led to designing many circuits and systems using MOSFETs operating in the subthreshold region. As an example, today medical and wireless applications, requiring ultra low power dissipation with low-to-moderate performance (10kHz-100MHz), are designed using this approach. Another example is the sensory information processing systems in wireless sensor networks. These systems employ MOSFETs operating in subthreshold region to minimize power dissipation and increase the life time of the battery. Recently, current-mode circuits employing MOSFETs working in the subthreshold region have been used to implement high performance contrast sensitive silicon retina.

1.4 Why Current-Mode Operation

The need for low voltage and low power designs for portable operation of electronic systems and biomedical instruments is highly required. Current-input current-output circuits are more attractive than their voltage-mode counterparts in such applications where low power consumption and long battery life are key factors. The reason is if the input and output signals are currents, then the circuit performance is completely determined by currents and the voltage levels are irrelevant in determining the performance. Usually, the nodes inside current mode circuits are low-impedance nodes. Thus, the voltage swings are usually small and, therefore, operation from low-voltage supplies is feasible. With low impedance nodes, the time constant of the circuits is relatively low and this results in wide bandwidth circuits. Moreover, in current mode circuits high gain is mostly not required. This results in simpler hardware structures. This justifies the growing range of applications of current mode circuits; for example, in neural networks, microwave and optical systems, continuous time filters and sampled data filters [6].

1.5 Operation of MOSFET devices at Different Inversion Levels

MOSFET devices in amplifier stages typically operate in their active (saturation) regions. However, within the active region a device may be biased to the strong inversion region, the moderate inversion region, or the weak inversion region. In weak inversion, the number of free carriers in the channel is small enough to lead to negligible drift current, but diffusion current flows as the MOSFET operates more like a bipolar junction transistor [7]. The gate-to-source voltage is near the threshold voltage and very small channel current densities exist in this situation. As gate-to-source voltage increases, more carriers are induced in the channel and drift current becomes more significant. In the moderate inversion region, drift and diffusion components are comparable. Strong inversion is reached as the gate-to-source voltage increases to the point that drift current dominates the drain current.

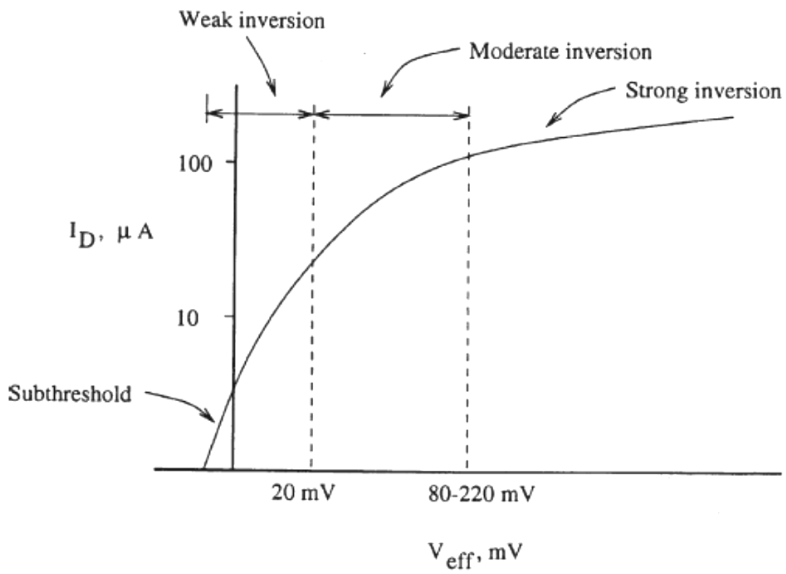


Figure 1.1 Drain current as a function of effective voltage [7]

A. Strong Inversion Region

The strong inversion region is perhaps the most commonly used among the three regions. Basic circuit design courses often confine discussion of MOSFET circuits to operation in this region since analytic equations are readily available. In the strong inversion region, variation of drain current with gate-to-source voltage is given by [7]

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} [V_{GS} - V_{th}]^2 [1 + \lambda (V_{DS} - V_{DSP})] \qquad (1.1)$$

Where V_{th} is the nominal threshold voltage, λ is the channel length modulation factor, and V_{DSP} is the drain-to-source pinchoff voltage.

B. Moderate Inversion Region

As V_{eff} ($V_{eff} = V_{GS} - V_{th}$) increases, more carriers are induced in the channel and drift current becomes more significant. In this region, drift and diffusion currents are comparable. Increased gate-to-source voltage leads to the strong inversion region when drift current dominates the diffusion component. Although an inversion coefficient can be defined to characterize the level of inversion [7], it can be approximately defined by the gate-to-source voltage. The lower end of the weak inversion region is the subthreshold region that exists for values of V_{GS} less than V_{th} when positive drain current flows. As V_{GS} ranges from subthreshold values up to about 20 mV above V_{th}, the device is in the weak inversion region. From a value of 20 mV above V_T to a V_{GS} of approximately 220 mV the device operates in the moderate inversion region [7]. Above this value of V_{GS} drift current dominates and the device is in the strong inversion region.

C. Weak Inversion Region

Weak inversion mode is the region when a MOSFET transistor gate-to-source voltage V_{GS} is below the threshold voltage V_{th}. Whereas the drain current has a near-square law variation in the strong inversion region, the approximate relation between drain current and gate-to-source voltage in the weak inversion region is given by [7]

$$I_{DS} = I_{Do} e^{\left(\frac{V_{GS}-V_{th}+(n-1)V_{BS}}{nV_T}\right)} \left[1 - e^{\left(-\frac{V_{DS}}{V_T}\right)}\right] \tag{1.2}$$

where $I_{Do} = 2nk_n'\frac{W}{L}V_T^2$ is the leakage current of the MOSFET, V_{GS} is the gate-to-source voltage, V_{th} is the threshold voltage of the MOS transistor, n ($1 \leq n \leq 3$) is the weak inversion slope factor, $V_{BS}$is the body-source voltage, and $V_T = \frac{KT}{q}$ is the thermal voltage (≈25mV at room temperature). K is Boltzmann constant ($1.38 * 10^{-23}\ {}^{J}/_{\circ K}$), T is temperature in degree Kelvin and q is charge of an electron ($1.6 * 10^{-19}$C), $k_n' = \mu_n C_{ox}\left(\frac{A}{V^2}\right)$ is the process transconductance parameter ($k_n = k_n'\frac{W}{L}\left(\frac{A}{V^2}\right)$), μ_n is the mobility of charge carriers$\left(\frac{cm^2}{V.s}\right)$, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_r\epsilon_o}{t_{ox}}$ is the normalized oxide capacitance (capacitor per unit gate area $\left(\frac{F}{m^2}\right)$), ϵ_{ox} is the permittivity of the silicone oxide $\left(\frac{F}{m}\right)$, t_{ox} is thickness of the oxide layer (m) and $\frac{W}{L}$ is the transistor aspect ratio.

If $V_{DS} \gg V_T$ and $V_{BS} = 0$, then equation (1.2) can be rewritten as follows:

$$I_{DS} = I_{Do}e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)} \tag{1.3}$$

As MOSFET integrated circuit technology has evolved to exploit smaller and smaller device structures, it has become increasingly important in recent years to look more closely at the minority carriers present under the gate when the gate-to-source voltage is less than the threshold voltage, i.e. in what is called the “sub-threshold” region. These carriers cannot be totally neglected, and play an important role in device and circuit performance. At first they were viewed primarily as a problem, causing undesirable “leakage” currents and limiting circuit performance. Now it is recognized that they also enable a very useful mode of MOSFET operation, and that the sub threshold region of operation is as important as the traditional cut-off, linear, and saturations regions of operation [9].

1.6 Literature Review

Over the last decade researchers have looked for implementation of known functions using MOSFET in weak inversion region such as non-linear functions, e.g. logarithmic and exponential, and computational functions like multiplier, divider, squarer and square rooter. They have looked for the low-voltage and low-power (LVLP) configurations so that it can be proper for many battery powered applications like Short Range Wireless and biomedical applications.

Operating the MOSFETs in subthreshold region is one approach to achieve low voltage and low power design. However, in the past, CMOS circuits using MOSFETs operating in subthreshold region have been inadequate for high speed applications, but have been used in applications that require ultra low power dissipation. With technology scaling, power supply and threshold voltage continue to decrease to simultaneously satisfy high performance and low power requirements. This leads to designing many circuits and systems using MOSFETs operating in subthreshold region. As an example, medical and wireless applications, require ultra low power dissipation with low-to-moderate performance (10 kHz-100MHz) are designed using this approach [10]. A current-mode exponential circuit using MOSFETs in weak inversion region was reported in [11]. This circuit approximates the exponential function through Taylor's series. Then, it has been concluded that it is power efficient. The supply voltage is 1V and the power consumption is 3.5uW. On the other side, the drawback of this circuit is the limited output range (with the reference I_B=300 nA, I_{out} varies from 1.37I_B to 3.65I_B, the output dynamic range is limited to 8.5dB). Another exponential function based on MOS transistors operating in the weak inversion region is presented in [12]. The proposed circuit has the advantage of being simple and small size (i.e. number of transistors). In [13] a new current-mode analog circuit configuration that implements the logarithmic function using BJT is proposed. The major advantage of this circuit realization compared to previously published circuits is that it can perform the logarithmic function for whatever of input greater or smaller than unity. A new Low-Voltage Low-Power (LVLP) CMOS current-mode circuit that performs divide and 1/x functions is reported in [14]. 1V power supply has been used. The disadvantage of this circuit is that the input signal can't be negative.

CMOS current-mode n^{th}-root circuit with only six transistors has been proposed in [15]. The input current-range is very wide from 120nA to 40uA with relative errors less than 1% for n greater than 2.

Gilbert in 1975 [16] has developed the Translinear Principle (TL) which is very useful in today's electronics area. Many researchers have implemented a variety of circuits based on this principle, mainly using BJTs and also MOS transistors in strong as well as weak inversion regions see for example [17],[18]. In [19], family of very low-power and low voltage analog building blocks that are based on MOSFET translinear loops has been presented. However the major drawbacks of these circuits are the effects of device mismatches and the limited gate-bulk operating voltage. In [20] analytical framework of CMOS translinear circuits in the subthreshold MOSFET has been presented. Among the few literatures reported, a current-mode squarer/divider circuit is proposed in [21] based on CMOS translinear loop. However the circuit operates at 1.5 V and consumes 150µW power. Square root circuit discussed in [22] is a typical example of classical exploitation of TL principle using BJTs. Though dynamic range of the circuit is high, due to device mismatch some appreciable errors are observed in output current. In [23] and [24] squaring circuit using MOSFETs in strong inversion has been presented. In strong inversion the current-voltage relationship is quadratic in nature and not exponential like in subthreshold and as a result their implementation yield an output current expression with additional terms along the required square function.

1.7 Problem Definition

From the literature review it appears that the logarithmic, exponential and computational circuits are important blocks and widely used in designing various analog systems. The drain-to-source current in MOSFET operating in weak inversion region, I_{DS} in equation (1.3), is strongly dependent on temperature and process variation and, is additionally, exponentially proportional to the voltages differentiate $(V_{gs} - V_{the})$. It is the aim of this thesis to design and simulate CMOS current-input current-output logarithmic and exponential functions meet the low voltage and low power requirements while they simultaneously feature the attractive characteristics of simplicity, only MOSFETs used, high accuracy and insensitive to temperature variation. To verify the efficiency of these functions different analog signal processing systems like variable gain-amplifier and computational circuits will be developed based on these cells. The attractive properties of log-antilog make them powerful to perform multiple functions in terms of programmability instead of designing different circuits and then additional circuit will be needed for programmability. Figure (1.2) illustrates the proposed architecture.

1.8 Thesis organization

The thesis work is presented as follows. In Chapter 2 Logarithmic and Exponential circuits are introduced and discussed as core cells. Chapter 3 presents new types of variable-gain attenuator, namely logarithmic-control variable-gain attenuator (LCVGA), and exponential-control variable-gain amplifier with extended output dB-linear range. Chapter 4 presents the proposed log-antilog based analog computational circuits to perform multiplication, division, squaring, inverse and cube-law functions. The conclusions and suggestions for future work are discussed in Chapter 5.

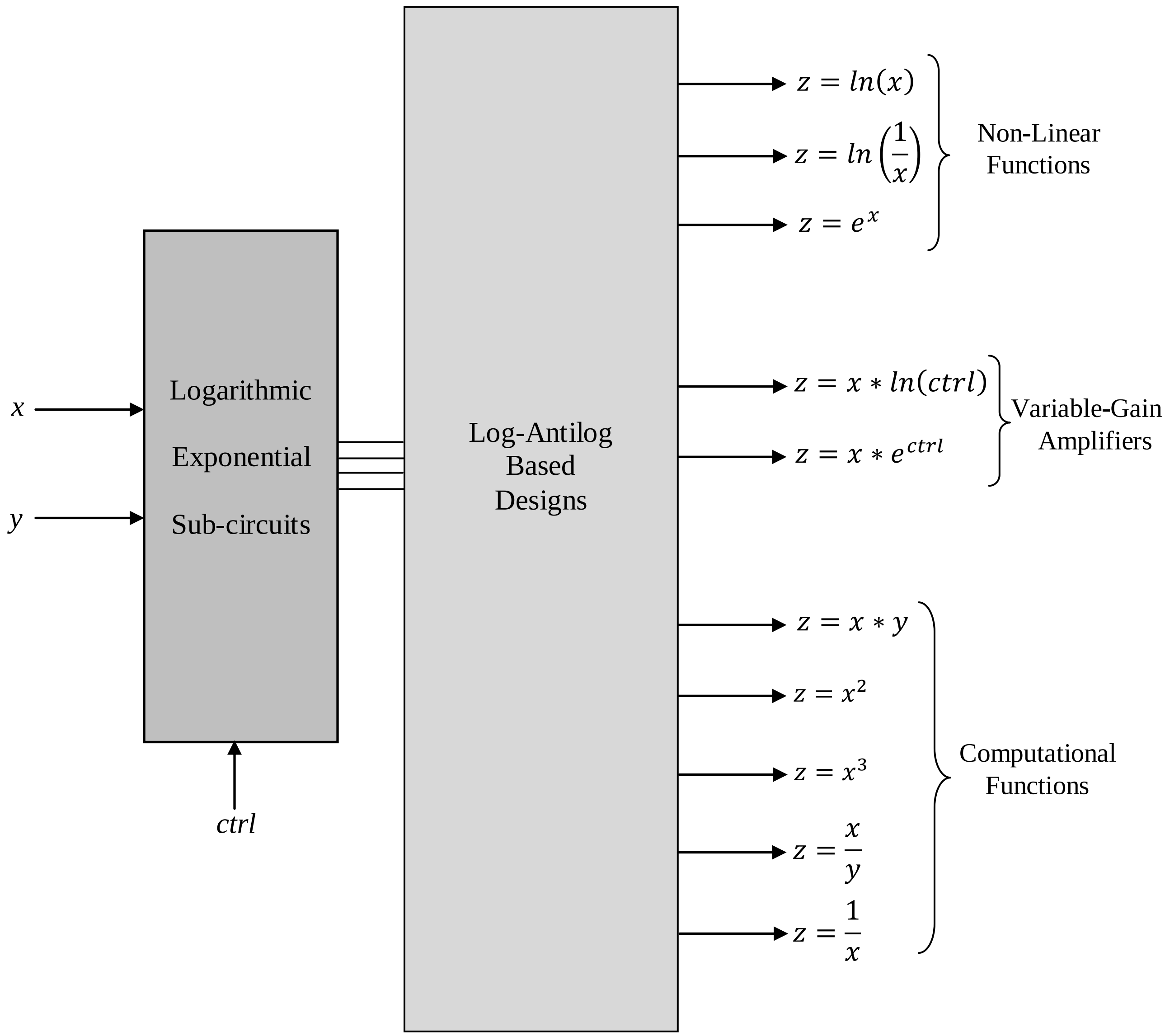


Figure 1.2 Proposed analog functions realizations using the Log-Antilog circuits

CHAPTER 2

CMOS CURRENT-MODE LOGARITHMIC AND EXPONENTIAL FUNCTIONS

2.1 CMOS Logarithmic Function Circuit

2.1.1 Introduction

Logarithmic amplifier is a non-linear device that produces an output that is proportional to the logarithm of the input. In certain applications, a signal may be too large in magnitude for a particular system to handle. In such cases, the signal voltage/current must be scaled down by a process called signal compression so that it can be properly handled by the system. If a linear circuit is used to scale down the amplitude of the signal, the lower voltages/currents are reduced by the same percentage as the higher voltages/currents. Linear signal compression often results in lower voltages /currents becoming obscured by noise and difficult to accurately distinguish. To overcome this problem, a signal with large dynamic range can be compressed using a logarithmic circuit. In logarithmic signal compression the higher voltages/currents are reduced by a greater percentage than the lower voltages, thus keeping the lower voltage/current signals from being lost in noise [25]. Figure (2.1) shows the basic concept of the signal compression with linear and logarithmic systems.

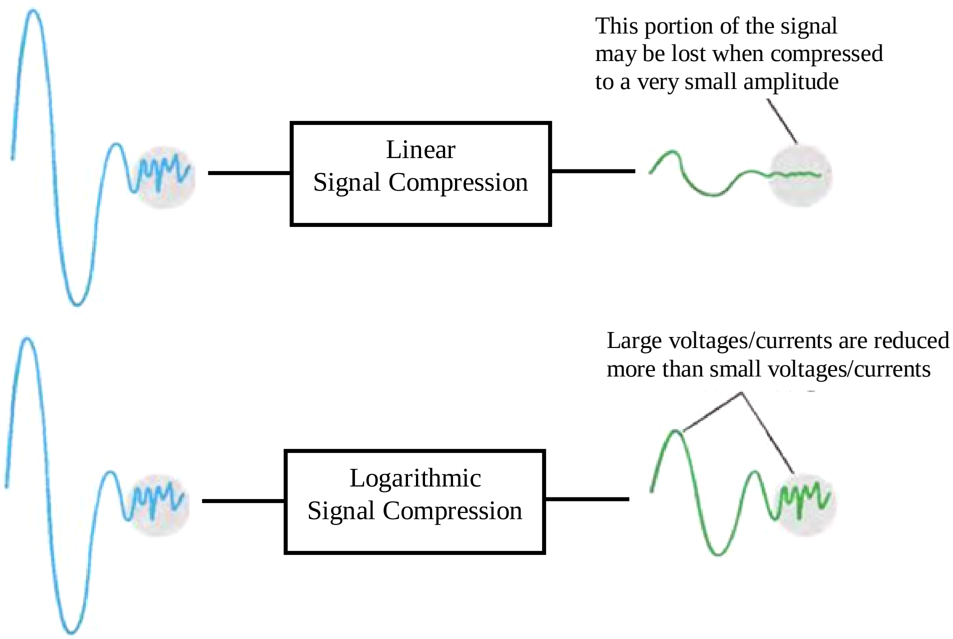


Figure 2.1 The basic concept of signal compression with a logarithmic amplifier

Moreover, the circuits that perform such characteristics are also widely used in many other applications; for example, medical equipment, instrumentation, telecommunication, active filters, disk drives, neural networks, applications that require compression of analog input data, linearization of transducers that have exponential outputs, and analog multiplication and division. This explains continuous interest in developing logarithmic function circuits manifested by the relatively large number of publications in this area; see for example Refs. [26–32] and the references cited therein. However, all these realizations have at least one of the following drawbacks:

- Absence of low voltage operation capability [26, 28, 30]
- Limited dynamic range [26, 27, 28, 31]
- Employment of BJT transistors [26, 30, 31]

- Doesn't enjoy Current-Mode operation [26, 28, 29, 31]
- Cannot realize a true logarithmic function circuit where the ratio is larger or smaller than unity [26, 27, 31, 32]
- Temperature dependent [26, 28-32]
- Relatively high power consumption [31, 32]
- No controllability [26, 27, 28, 31]
- To some extent, linearity error is high [28, 31, 32]
- Use passive elements i.e. resistors [26, 27, 30, 31]
- Complexity [31, 32]

In the most recent published works [26-28], voltage-mode logarithmic converter is presented [26] and voltage-current logarithmic circuit is reported in [28]. However, these two realizations are temperature dependent. Current-mode logarithmic function generator was presented in [27]. This circuit can realize a logarithmic function of the form:

$$I_{out} = \frac{I_{b4}}{ln(N)} ln\left(\frac{I_{in}}{I_{b2}}\right)$$

Where N (the ratio between the biasing currents) is a constant, I_{out} is the output current, I_{b2} and I_{b4} are biasing currents and I_{in} is the input current. However, since I_{out} must be positive, then the condition $I_{in} \geq I_{b2}$ must be satisfied. Thus, the circuit cannot realize a true logarithmic function circuit where I_{in} and I_{b2} can attain arbitrary positive values and I_{out} can attain any positive or negative value.

The major intention of this work is, therefore, to develop a current-input current-output circuit capable of performing $Log(x)$ and $Log(1/x)$ in CMOS technology for any value of x larger or smaller than unity, working under low voltage supply and consumes low power while it simultaneously features with simplicity, good accuracy, temperature independent.

2.1.2 First Proposed Design

A new scheme for a controllable CMOS low-voltage and low-power current mode logarithmic function circuit is introduced. The proposed design absorb normalized input range (27.1dBm), has controllable output amplitude, high accuracy and insensitive to temperature variation (0.036nA/1℃), while it simultaneously features the attractive characteristics of simplicity, operates under very low power supply (±0.5V), and consumes an ultra low power (0.3µW). The functionality of the proposed topology is confirmed using HSPICE with 0.35µm CMOS process.

2.1.2.1 Design Principle

Based on Taylor's series expansion, the exponential function can be approximated as expressed below:

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots + \frac{x^n}{n!} + \cdots \qquad (2.1)$$

Where x is the independent variable and If x is much smaller than one ($x \ll 1$), then the higher order terms in Taylor's approximation can be neglected and (2.1) can be written as:

$$e^x \approx 1 + x + \frac{x^2}{2!} \quad if\ x \ll 1 \qquad (2.2)$$

According to equation (2.2), one can write

$$e^{-x} \approx 1 - x + \frac{x^2}{2!} \quad if\ x \ll 1 \qquad (2.3)$$

Subtracting equation (2.3) from equation (2.2) we can easily get:

$$e^x - e^{-x} = 2x \quad if\ x \ll 1 \tag{2.4}$$

The error between "$e^x - e^{-x}$" and "2x" is plotted in figure (2.2). The error can be less than 0.1% while the input variable $|x| < 0.2$.

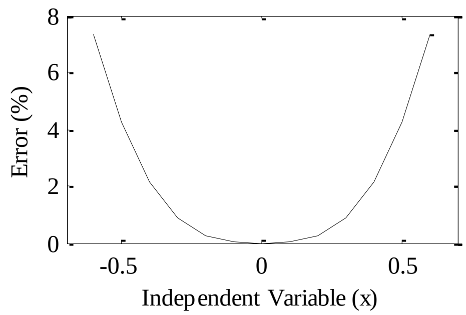


Figure 2.2 Error between "$e^x - e^{-x}$" and "2x"

With reference to the exponential function generator cell shown in figure (2.3) where I_b is the bias current [33-34], and assuming that both M1 and M2 are perfectly matched and both of them are biased in the weak inversion region, using equation (1.2) and assuming $V_{DS} \geq 4V_T$, the currents I_b and I_2 can be expressed as [35]

$$I_b = I_{D0} \cdot \exp\left[\frac{(V_{DD} - V_A) + (n-1)V_{BS}}{nV_T}\right] \tag{2.5}$$

and

$$I_2 = I_{D0} \cdot \exp\left[\frac{(V_{DD} - V_B) + (n-1)V_{BS}}{nV_T}\right] \tag{2.6}$$

From equations (2.5) and (2.6) we will get

$$I_2 = I_b \cdot \exp\left[\frac{(V_A - V_B)}{nV_T}\right] \tag{2.7}$$

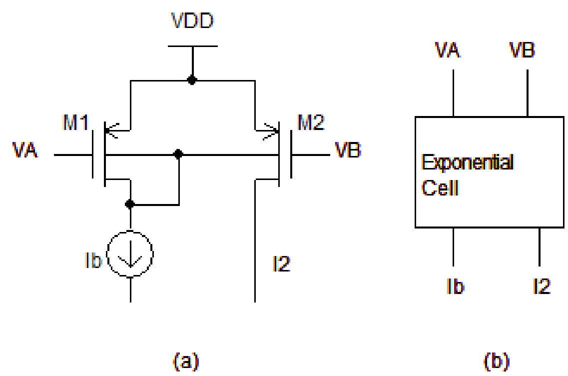


Figure 2.3 Basic exponential function circuit (a) Circuit (b) Symbol [33]

2.1.2.2 Proposed Design

The block diagram of the proposed current-mode logarithmic circuit is shown in figure (2.4). The transistor level and layout of the proposed design is shown in figure (2.5) (a) and (b) respectively. With reference to figure (2.5), the current I_b is the bias current, I_x and I_y are the two input current signals and I_{out} is the output current.

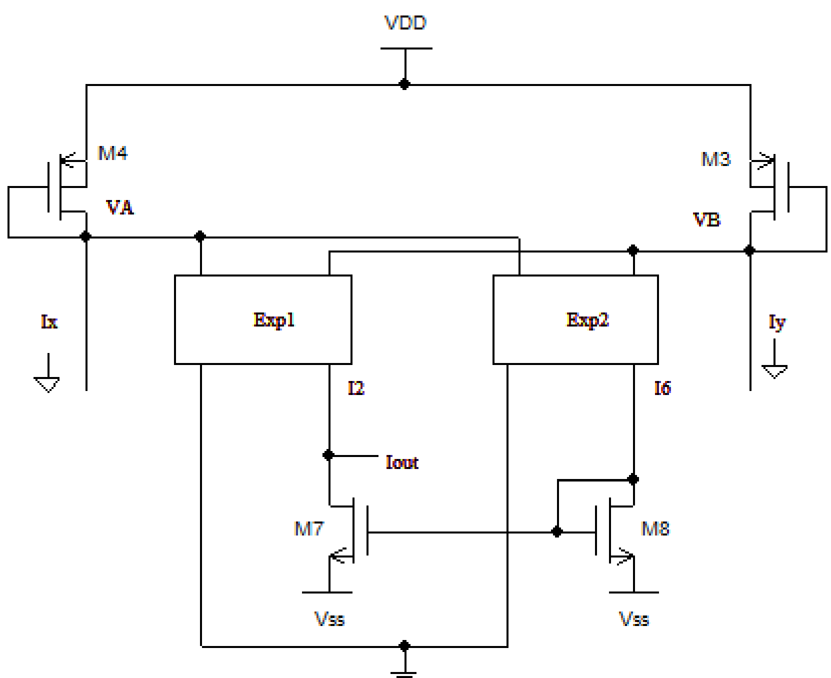
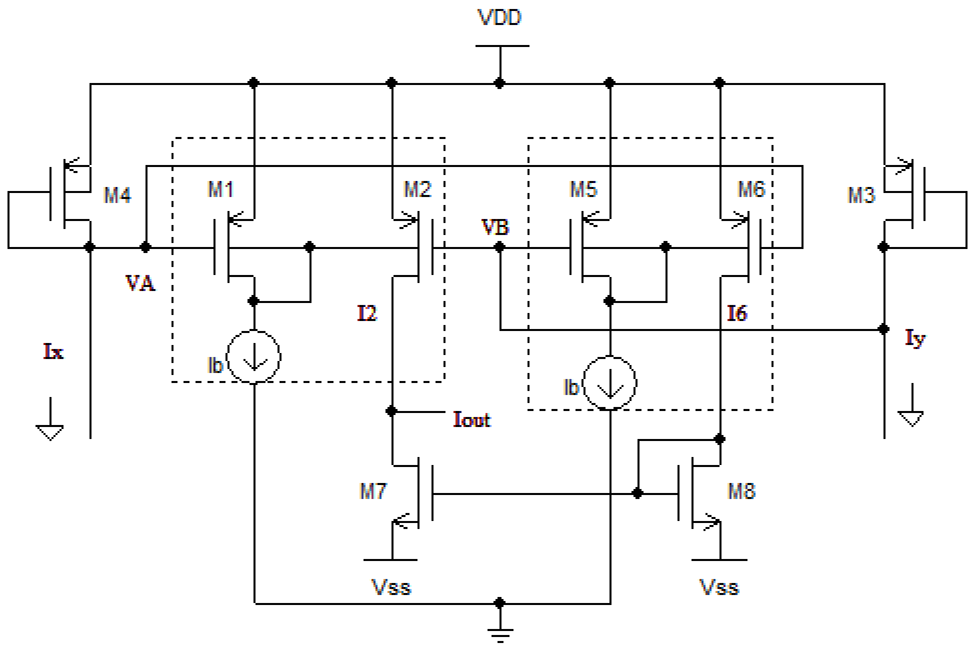
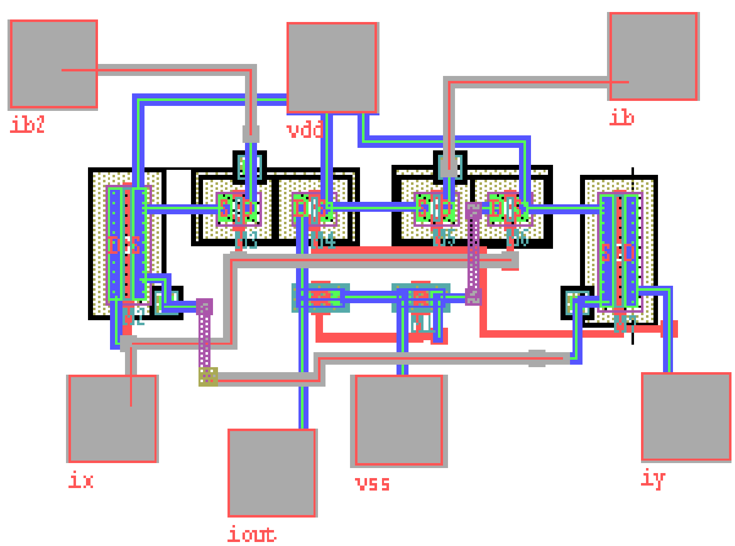


Figure 2.4 Block diagram of the proposed logarithmic circuit design



(a)



(b)

Figure 2.5 Proposed logarithmic circuit (a) transistor level (b) post-layout

The drain currents in transistors M_2 and M_6 are given by:

$$I_2 = I_b \cdot \exp\left[\frac{(V_A - V_B)}{nV_T}\right] \tag{2.8}$$

$$I_6 = I_b \cdot \exp\left[\frac{(V_B - V_A)}{nV_T}\right] \tag{2.9}$$

Equation (2.9) can be rewritten as:

$$I_6 = I_b \cdot \exp\left[\frac{-(V_A - V_B)}{nV_T}\right] \tag{2.10}$$

The drain current for transistor M_8 is the same as the drain current I_6

$$I_{out} = I_2 - I_8 = I_2 - I_6 \tag{2.11}$$

From (2.8), (2.10) and (2.11), the output current is given by:

$$I_{out} = I_b\left[\exp\left[\frac{(V_A - V_B)}{nV_T}\right] - \exp\left[\frac{-(V_A - V_B)}{nV_T}\right]\right] \tag{2.12}$$

Using equation (2.4) and with the term $\left[\frac{(V_A - V_B)}{nV_T}\right] \ll 1$, it is easy to show that

$$I_{out} = 2I_b \cdot \left[\frac{(V_A - V_B)}{nV_T}\right] \tag{2.13}$$

Transistors M_3 and M_4 are used to convert the input currents I_y and I_x to voltages V_B and V_A respectively in logarithmic form as shown in equations (2.14) and (2.15), respectively:

$$V_A = V_{DD} - V_{sg4} = V_{DD} - nV_T ln\left(\frac{I_x}{I_{Do}}\right) - V_{th} \tag{2.14}$$

$$V_B = V_{DD} - V_{sg3} = V_{DD} - nV_T ln\left(\frac{I_y}{I_{Do}}\right) - V_{th} \tag{2.15}$$

combining equations (2.15) and (2.14) to get:

$$\left[\frac{(V_A - V_B)}{nV_T}\right] = ln\left(\frac{I_y}{I_x}\right) \tag{2.16}$$

Substituting equation (2.16) in (2.13); the output current I_{out} will be expressed by:

$$I_{out} = 2I_b ln\left(\frac{I_y}{I_x}\right) \tag{2.17}$$

Equation (2.17) implements a current-mode logarithmic function circuit. If the current I_x is kept constant, the output current I_{out} is proportional to the logarithm of I_y , and its gain can be adjusted by the bias current I_b. Since the transistors in figure (2.5) are biased in the weak inversion region, the power consumption of the proposed circuit is very low. Moreover, in the proposed circuit, there are only two transistors stacked in the electric path between the voltage supply and the ground, therefore the proposed design is suitable for low supply voltage. To assure the MOSFET is operating in weak inversion forward saturation, $I_D \leq I_{Do}$ and $V_{DS} \geq 4V_T$ [35-37].

2.1.2.2.1 Mismatch Analysis

In real implementation there is always mismatch between the transistors. Referring to figure (2.5), assume that the threshold voltage of M3 and M4 are $V_{th} + |\Delta V_{th3}|$ and $V_{th} + |\Delta V_{th4}|$ and leakage currents are $I_{Do3} + |\Delta I_{Do3}|$ and $I_{Do4} + |\Delta I_{Do4}|$, then equations (2.14) and (2.15) can be rewritten as

$$V_A = V_{DD} - V_{sg4} = V_{DD} - nV_T ln\left(\frac{I_X}{I_{Do}+|\Delta I_{Do4}|}\right) - V_{th} + |\Delta V_{th4}| \tag{2.18}$$

$$V_B = V_{DD} - V_{sg3} = V_{DD} - nV_T ln\left(\frac{I_Y}{I_{Do}+|\Delta I_{Do3}|}\right) - V_{th} + |\Delta V_{th3}| \tag{2.19}$$

combining equations (2.18) and (2.19) to get

$$\frac{V_A - V_B}{nV_T} = ln\left(\frac{I_Y}{I_X}\right) + ln\left(\frac{I_{Do}+|\Delta I_{Do4}|}{I_{Do}+|\Delta I_{Do3}|}\right) + \left\{\frac{|\Delta V_{th4}| - |\Delta V_{th3}|}{nV_T}\right\} \tag{2.20}$$

according to equations (2.13) and (2.20), the output current can be rewritten as:

$$I_{out} = 2I_b ln\left(\frac{I_Y}{I_X}\right) + 2I_b ln\left(\frac{I_{Do}+|\Delta I_{Do4}|}{I_{Do}+|\Delta I_{Do3}|}\right) + 2I_b\left\{\frac{|\Delta V_{th4}| - |\Delta V_{th3}|}{nV_T}\right\} \tag{2.21}$$

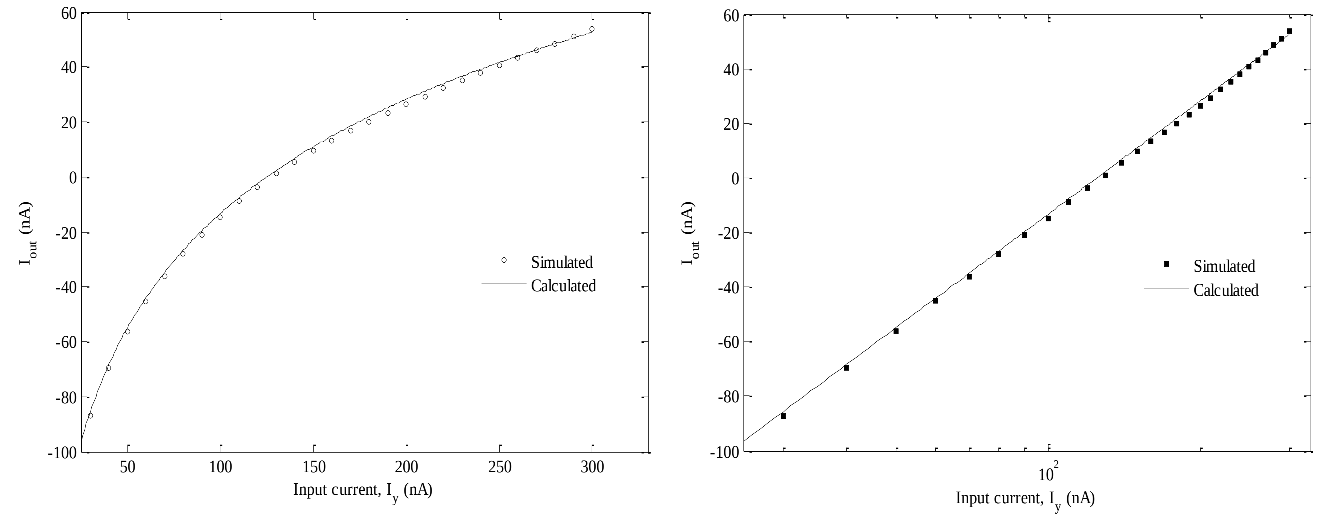
Inspection of equation (2.21) clearly shows that the output current of the logarithmic circuit comprises three current components. The desired component that is proportional to the logarithmic of the input current in addition to two undesired components. The two undesired components are constant current components.

2.1.2.3 Simulation Results

The developed circuit was simulated using HSPICE level 49 which is equivalent to EKV model in 0.35μm 2p4m CMOS process technology and the results were obtained with $I_b = 30nA$, $I_x = 125nA$ and V_{DD}=-V_{SS}=500 mV. The aspect ratios of transistors in figure (2.5) are listed in table (2.1). The output current was measured by forcing it through a grounded load resistor$R_L = 1k\Omega$. The simulated and calculated results are shown in figure (2.6). As the input current I_y varies from $20nA$ to $400nA$ (while$I_x = 125nA$), the measured output dynamic range is around $149nA$. It appears from figure (2.6) that the simulated results are in very good agreement with the required function which confirms the functionality of the developed design. It can be seen that at $I_y = 125nA$ the output current will be Zero.

Table 2.1 Dimension ratios of transistors of figure (2.5)

Transistor	**Aspect Ratios W/L μm/μm**
M1-M2	1.4/0.35
M3-M4	6.3/0.35
M5-M6	1.4/0.35
M7-M8	1/1



(a) (b)

Figure 2.6 Simulated and calculated results (a) linear scale (b) semi-log scale

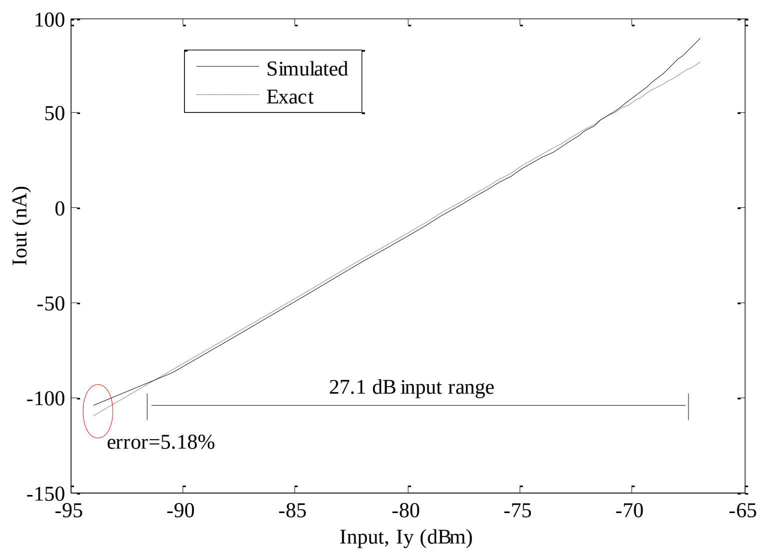


Figure 2.7 Log and transfer characteristic of the proposed design

Figure (2.7) shows the simulation results of the proposed design when the input current, I_y is normalized to a reference current equal to $1mA$.

The gain term 'I_b' was varied and the corresponding output response is shown in figure (2.8). As clearly seen in figure (2.8), the output current can be adjusted by the current I_b. The results also demonstrate that a larger output dynamic range can be obtained by increasing the current I_b.

The error between the simulated results and the theoretical values calculated by equation (2.17) is defined by the following formula:

$$error\% = \frac{simulated\ value - theoretical\ value}{theoretical\ value} \times 100\% \tag{2.22}$$

The maximum simulated error was 4% which occurred at normalized current $\frac{I_y}{I_x} = 1.36$ and $I_b = 30nA$; however most of the simulated errors are less than 4%. The simulated maximum power consumption for the proposed circuit is 0.284µW which happened at $I_x = 125nA\ and\ I_b = 30nA$.

The temperature independency of the proposed design has been confirmed, the temperature was varied from -25 to +75°C (i.e. 100℃ variation range) and the output current was monitored. The output current was normalized to its current at level +25°C and it appears from Figure (2.9) that I_{out} is insensitive to temperature variation. At I_y equal to 300nA, the output current I_{out} was 53.3nA, 53.72nA, and 54.82nA for T equal to -25℃, 25℃ and 75℃ respectively while the nominal value is 52nA. The maximum deviation from the nominal value is 2.82nA which happened at 75℃. In other words, the max deviation is 0.0376nA per 1℃ as illustrated below:

$$75°C \xrightarrow{yields} 2.82nA\ deviation$$

$$\therefore\ 1°C \xrightarrow{yields} x\ deviation$$

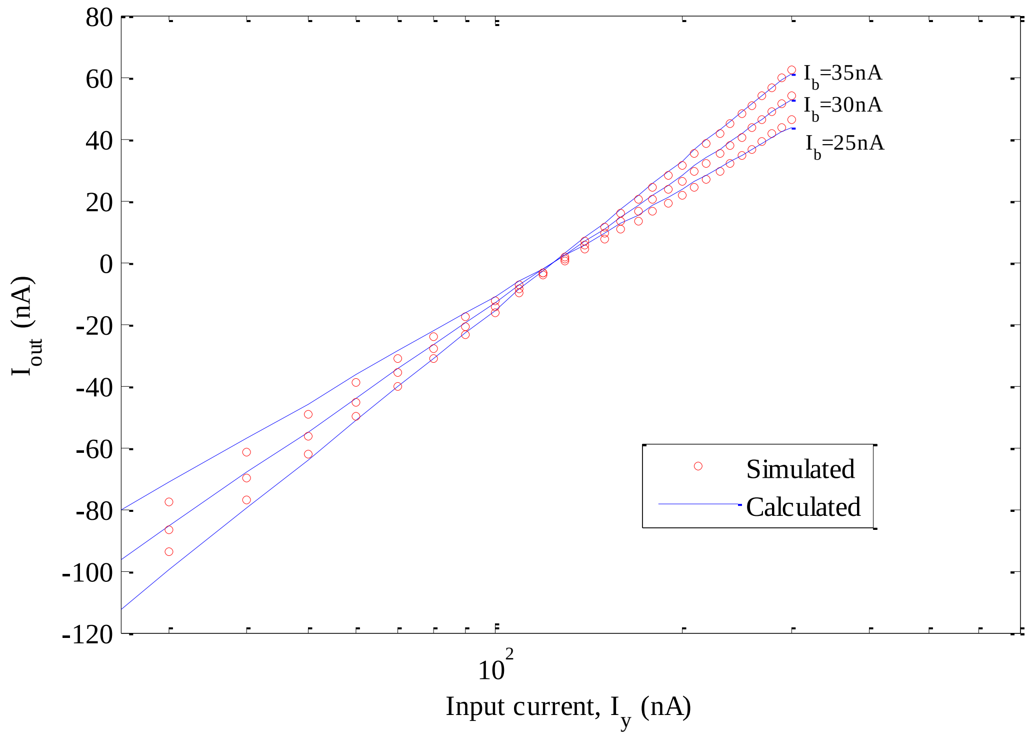
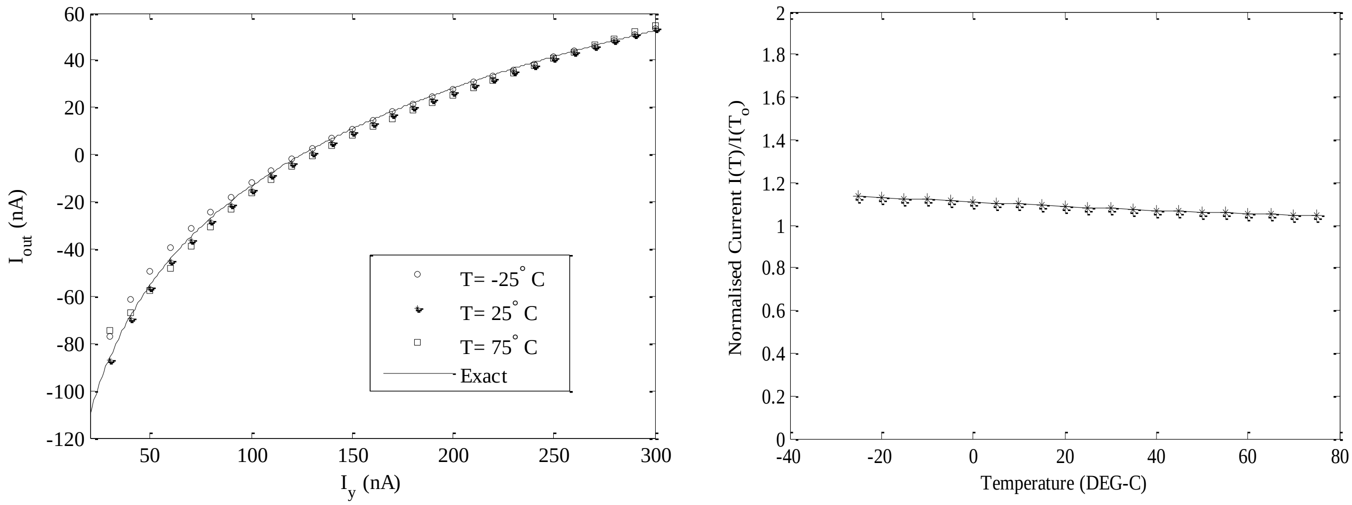


Figure 2.8 Varying the gain using the bias current I_b

Figure (2.10) shows the output current waveform for the triangular input wave signal of 280nA peak to peak and f=10 kHz. From figure (2.10) the functionality of the proposed design is confirmed. With reference to equation (2.17), in case of I_x is the input signal and I_y is kept constant then the $Log(1/x)$ function can be realized. Figure (2.11) shows the results. The circuit was also simulated for frequency response. The -3dB bandwidth is found to be 5.7MHz as shown in figure (2.12).

Table 2.2 summarizes the performance of the introduced logarithmic circuits (first and second designs) compared to the most recent published works.



(a) Before normalization

(b) After normalization

Figure 2.9 Simulation for temperature insensitivity

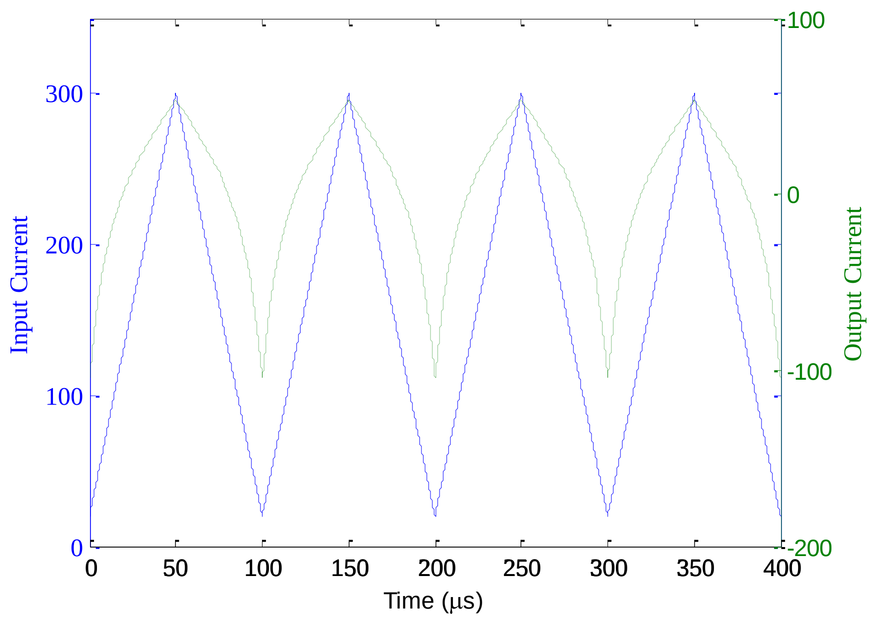


Figure 2.10 Triangular wave response

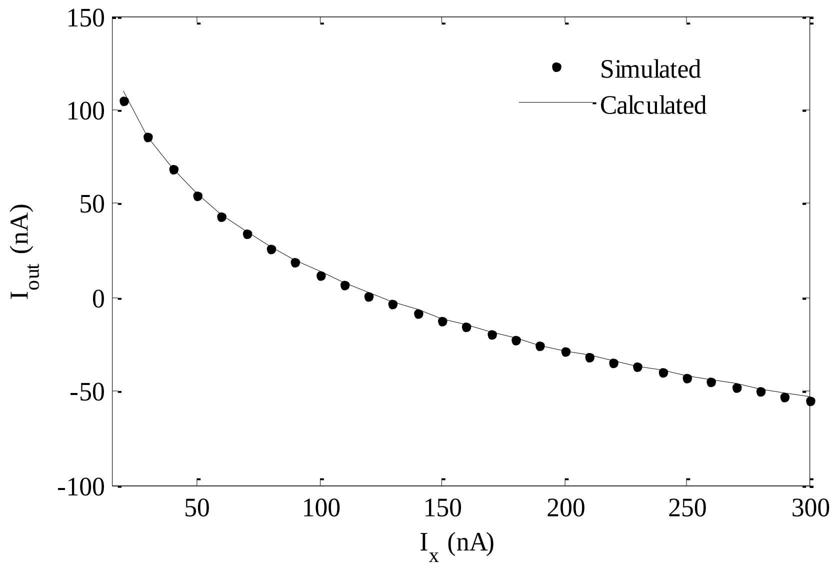


Figure 2.11 Results of the $Log(1/x)$ relization

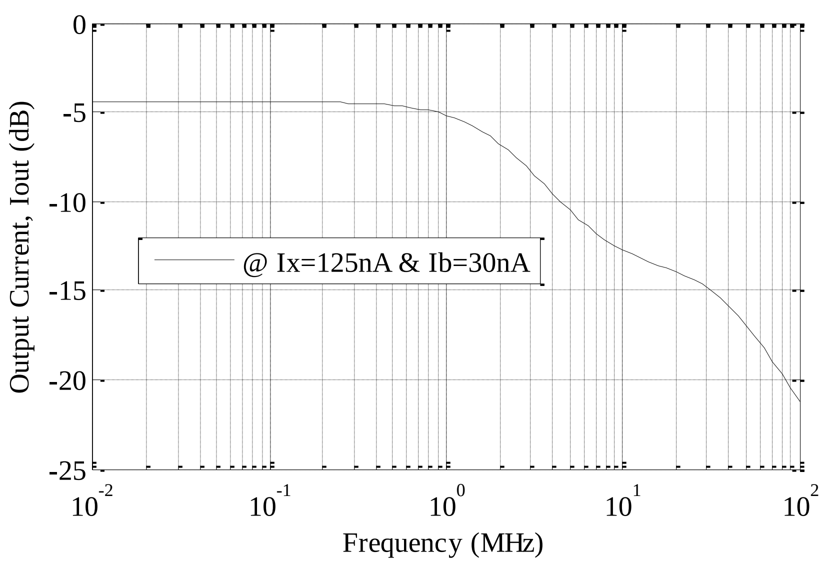


Figure 2.12 Frequency response

2.1.2.4 Discussion

In this design, a new logarithmic function circuit is proposed. The circuit enjoys attractive features at once. It offers highly accurate logarithmic function of the form of equation (2.17) for any value of I_Y larger or smaller than I_X. The introduced design is good for integration since it uses only MOSFET transistors. The performance of the proposed logarithmic circuit has been verified using HSPICE tool and with 0.35 μm process, where both controllability and temperature independency have been considered. The circuit consumes around 0.3μW and has less than 4% linearity error. The proposed low-voltage and low-power circuit is expected to be useful in many analog signal processing applications. When the current I_Y is increased, the simulated error is also increased. One of the reasons is due to the neglect of the higher order terms in equation (2.1). Another reason is that the larger I_Y will results in larger V_{sg3} and larger V_{sg3} will drive the MOS_3 transistor into strong region; therefore the V-I characteristics can no longer be exponential.

Table 2.2 Performance comparison

Parameter	Performance			
	[26]	[27]	[28]	This work
Process	0.18µm BiCMOS	0.5µm CMOS	0.18µm CMOS	0.35μm, 2p4m CMOS
No. of transistors	9 (2 BJT)	21	4	8
Passive elements e.g. R & C	Two resistors	Two resistors	Non	Non
Operation Region	Active (BJT)	Weak inversion	Weak inversion	Weak inversion
Voltage Supply (V)	> 1.3	——	1.8	±0.5
Input\output	Voltage\ voltage	Current\ current	Current\ voltage	Current\current
Max. linearity error	36dB (63%)	NA	5%	4%
Power dissipation (µW)	17750	NA	0.3	0.284
Gain controllability	No	Yes	No	Yes
True for $x \geq 1$ $or <$ 1?	Not satisfied	Not satisfied	Satisfied	Satisfied
Temperature	Dependent	Compensated using a PTAT* and resistive cancellation technique	Dependent	Independent
Area	NA	NA	NA	16um x 18um

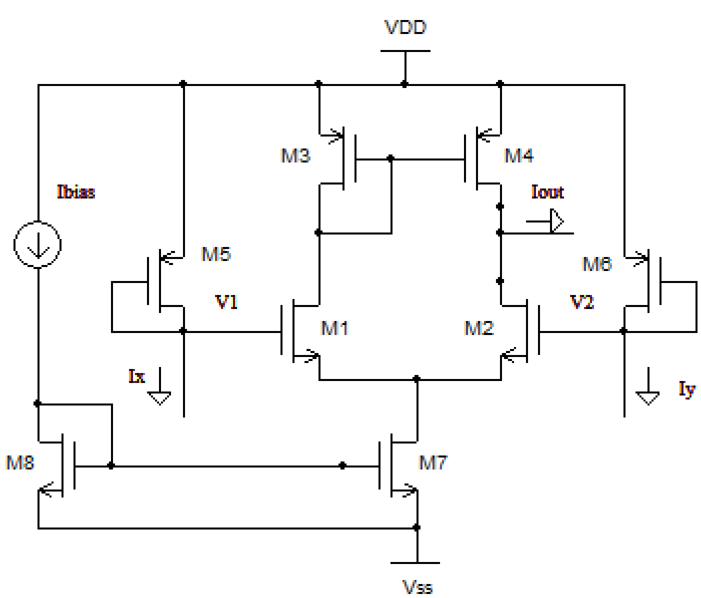
**Proportional-to-absolute- temperature (PTAT)

2.1.3 Second Proposed Design

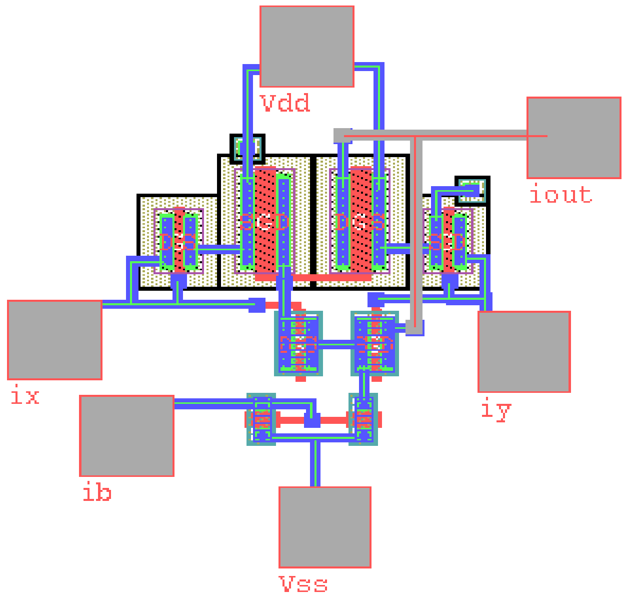
A novel CMOS current-mode controllable low-voltage and low-power logarithmic function circuit is introduced. It consists of one Operational Transconductance Amplifier (OTA) and two PMOS transistors biased in weak inversion region. The proposed design provides high dynamic range, controllable amplitude, high accuracy and it is insensitive to temperature variation. The circuit operates from ± 0.75V power supply and consumes 0.5µW. The functionality of the proposed circuit was verified by simulation using HSPICE with 0.35µm 2p4m CMOS process.

2.1.3.1 Proposed OTA-Based Design

The proposed design concept is shown in figure (2.13) (a). It consists of an Operational Transconductance Amplifier (OTA) and two PMOS transistors, M5 and M6 biased in weak inversion region. The physical layout is shown in figure (2.13), (b).



(a)



(b)

Figure 2.13 Proposed Circuit (a) Transistor level (b) Physical-Layout

It is well known that the output current of the OTA is given by:

$$I_{out} = g_m(V_1 - V_2) \tag{2.23}$$

where g_m is the transconductance of the MOSFET pair used in the OTA, V_1 and V_2 are the OTA's two input voltages. Transistors M5 and M6 are biased in weak inversion region and are used to convert the input currents I_x and I_y to voltages V_1 and V_2 respectively in logarithmic form as shown in equations (2.24) and (2.25) respectively:

$$V_1 = V_{DD} - V_{sg5} = V_{DD} - nV_T \ln\left(\frac{I_x}{I_{Do}}\right) - V_{th} \tag{2.24}$$

$$V_2 = V_{DD} - V_{sg6} = V_{DD} - nV_T \ln\left(\frac{I_y}{I_{Do}}\right) - V_{th} \tag{2.25}$$

Where V_1 and V_2 are the input voltages of M1 and M2 respectively, V_{DD} is the supply voltage, V_{sg} is the source-to-gate voltage.

Combining equations (2.24) and (2.25) yields:

$$(V_1 - V_2) = nV_T \ln\left(\frac{I_y}{I_x}\right) \tag{2.26}$$

Combining (2.26) and (2.23), one can easily get the output current I_{out} expressed by:

$$I_{out} = g_m nV_T \ln\left(\frac{I_y}{I_x}\right) \tag{2.27}$$

The transconductance g_m of the transistor in weak inversion region is given by:

$$g_m = \frac{I_D}{nV_T} \tag{2.28}$$

where I_D is the drain current of MOSFETs M1 and M2 and is given by:

$$I_D = \frac{I_{bias}}{2} \tag{2.29}$$

From (2.27), (2.28) and (2.29) the output current can be written as:

$$I_{out} = \frac{I_{bias}}{2} \cdot \ln\left(\frac{I_y}{I_x}\right) \tag{2.30}$$

With reference to equation (2.30), if the current I_x is fixed, the output current I_{out} is proportional to the logarithm of the input current I_y and if I_y is kept constant, then the function log $(1/x)$ can be realized. The amplitude of the output current can be scaled by varying the current I_{bias} of the OTA. As shown in figure (2.13) (a), the transistors M1-M4 form the OTA and M7-M8 provide the required bias current. Since M1-M6 are biased in the weak inversion region, the power consumption can be very low. Besides, there is only three transistors cascoded in the supply voltage path; it can operate under low supply voltage.

2.1.3.2 Second order effects

The characteristic of the logarithmic circuit in figure (2.13) was obtained by assuming transistors are perfectly matched. In real implementation there is always mismatch between the transistors in addition to the body effect error.

A. Mismatch analysis

If the transconductance, g_m, where $\left(g_m = \frac{I_D}{nV_T} = \frac{2nK_{p,n}\frac{W}{L}V_T^2 \cdot e^{\left(\frac{V_{gs}-V_{th}}{nV_T}\right)}}{nV_T} \right)$ of the transistors M1-M2 of the proposed logarithmic circuit is not perfectly matched due to a non identical slope factor (n) or mismatched aspect ratios $\left(\frac{W}{L}\right)$ -which directly proportional to the g_m- due to process variation, for example, the transconductance of M1 and M2 is $g_m + \Delta g_{m1}$ and $g_m + \Delta g_{m2}$ respectively; then equation (2.23) can be derived again as

$$I_{out} = g_m(V_1 - V_2) + \{\Delta g_{m1}(V_1) - \Delta g_{m2}(V_2)\} \tag{2.31}$$

According to equation (2.31), and by recalculating equations (2.24)-(2.29), equation (2.30) can be rewritten as

$$I_{out} = \frac{I_{bias}}{2} ln\left(\frac{I_Y}{I_X}\right) + \{\Delta g_{m1}(V_1) - \Delta g_{m2}(V_2)\} \tag{2.32}$$

$$|I_{error}| = \{\Delta g_{m1}(V_1) - \Delta g_{m2}(V_2)\} \tag{2.33}$$

From equation (2.32), it is clear that a current error deviation is generated.

Moreover, assuming there is threshold voltage,V_{th} mismatched between M5 and M6, where$V_{th5} = V_{th} + \alpha$ and $V_{th6} = V_{th} - \alpha$, respectively then equation (2.26) will be

$$V_1 - V_2 = \mathrm{nU_T ln}\left(\frac{\mathrm{I_y}}{\mathrm{I_X}}\right) + 2\alpha \tag{2.34}$$

and then recalculate equations (2.24)-(2.29), the equation (2.30) can be rewritten as

$$I_{out} = \frac{I_{bias}}{2} ln\left(\frac{I_Y}{I_X}\right) + \frac{\alpha I_{bias}}{nU_T} \tag{2.35}$$

$$|I_{error}| = \frac{\alpha I_{bias}}{nU_T} \tag{2.36}$$

According to equation (2.35), the output current has two current components. The desired component that is proportional to the logarithmic of the input current in addition to undesired component. The undesired component is a constant current component.

Besides the transconductance and threshold voltage mismatch, the leakage current I_{Do} of the MOSFET in subthreshold region is proportional to the aspect ratio of the MOSFET, consequently, if the aspect ratios of M5–M6 in figure (2.13) are mismatched due to the process variation, it would result in the leakage current of M5–M6 to be not identical; i.e., $I_{Do5} = I_{Do} + \Delta I_{Do5}$ and $I_{Do6} = I_{Do} + \Delta I_{Do6}$, and by substituting these leakage currents into equations (2.24)-(2.25), respectively, and recalculate equations (2.27)-(2.29), as a result equation (2.30) can be obtained again as

$$I_{out} = \frac{I_{bias}}{2} ln\left(\frac{I_{in}}{I_x}\right) + \left\{\frac{I_{bias}}{2} ln\left(\frac{\mathrm{I_{Do}+\Delta I_{Do5}}}{\mathrm{I_{Do}+\Delta I_{Do6}}}\right)\right\} \tag{2.37}$$

Subtracting equation (2.30) from equation (2.37) we get the output current error quantity as

$$|I_{error}| = \left\{\frac{I_{bias}}{2} ln\left(\frac{\mathrm{I_{Do}+\Delta I_{Do5}}}{\mathrm{I_{Do}+\Delta I_{Do6}}}\right)\right\} \tag{2.38}$$

From equation (2.37) undesired component is generated.

To further investigate the mismatch effect, assuming that there is a ±10% variation of the aspect ratios between M5 and M6. After thirty times iterations, the Monte Carlo analysis indicates that, the corresponding maximum deviation is 4.74%.

B. Error due to body effect

In the MOSFET transistors, as the source-to-bulk voltage V_{SB} increases, the threshold voltage V_{th} will be also increased. This is called the "body effect", which can be characterized by

$$V_{th} = V_{th0} + \gamma\left[\sqrt{(2\emptyset_b + |V_{SB}|)} - \sqrt{2\emptyset_b}\right] \tag{2.39}$$

where V_{th0} is the zero body bias threshold voltage, γ is the bulk-threshold parameter (typical value of $0.7V^{-\frac{1}{2}}$) and $\emptyset_b$ is the surface-potential (typical value of 0.6V). To avoid this effect, the cascaded MOS transistors should be placed in separated wells, and thus V_{SB} will be zero. So, these transistors will have zero body bias threshold voltage. In M3→M8 transistors bulk is connected to the source, hence $V_{SB} = 0$ and $V_{th} = V_{th0}$, but in M1 and M2 transistors $V_{SB} \neq 0$. Considering this mismatch between M1 and M2 transistors where $V_{th1} = V_{th} + \beta,\ V_{th2} = V_{th} - \beta$ and β is the mismatch term between V_{th1} and V_{th2}, equation (2.23) can be rewritten as

$$I_{out} = g_m(V_1 - V_2) - g_m 2\beta \tag{2.40}$$

According to equation (2.40) and then recalculate equations (2.26)-(2.29), the equation (2.30) can be rewritten as

$$I_{out} = \frac{I_{bias}}{2} ln\left(\frac{I_Y}{I_X}\right) - \frac{\beta I_{bias}}{nU_T} \tag{2.41}$$

$$|I_{error}| = \frac{\beta I_{bias}}{nU_T} \tag{2.42}$$

Form equation (2.41), it is clear that the body effect will cause a deviation error. The amount of the deviation is indicated in equation (2.42). To prevent this deviation, the cascoded MOS transistors should be placed in separated wells.

2.1.3.3 Simulation Results & Discussion

The functionality of the proposed circuit was carried out using HSPICE tool where the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm two-polysilicon and four-metal layer (2p4m) CMOS processes was employed to simulate the circuit.

For the MOSFET to work in weak inversion forward saturation, the following two conditions must be satisfied [37],

$$\begin{cases} V_{DS} \geq 3V_T, & for\ NMOS \\ V_{SD} \geq 3V_T, & for\ PMOS \end{cases} \tag{2.43}$$

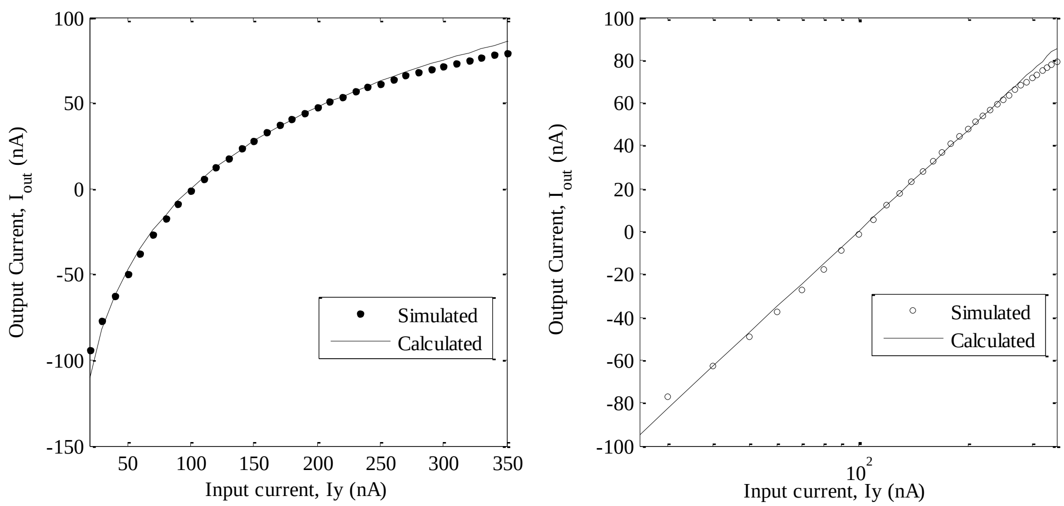
$$I_D < I_{Do} \tag{2.44}$$

The threshold voltage for the NMOS transistor is 0.582V and that for the PMOS transistor is −0.766V in our process and the voltage supply in the simulation is ±0.75V. To comply with equations (2.43) and (2.44), the aspect ratios of all transistors of the proposed logarithmic function circuit are listed in table (2.3) and the bias current can be set from 40nA up to 175nA.

Table 2.3 Summery of transistors dimensions of figure (2.13)

Transistor	**Aspect Ratio** $\frac{W(\mu m)}{L(\mu m)}$	**Ratios**
M1-M2	$^{3.5}/_{1.75}$	2
M3-M4	$^{3.5}/_{19.6}$	1/5.6
M5-M6	$^{21}/_{0.35}$	60
M7-M8	$^{14}/_{14}$	1

The simulated results are shown in figure (2.14) where the bias current $I_{bias} = 135nA$ (i.e.$I_D \simeq 68.5nA$), $I_x = 100nA$ and V_{DD}=-V_{SS}=0.75V. As the input current I_y varies from 20nA to 350nA (while$I_x = 100nA$), the measured output current range can be 173.1nA (from -93.83nA to 79.25nA). It appears from figure (2.14) that the simulated results are in very good agreement with the required function which confirms the functionality of the developed design. The output current was measured by forcing it through a grounded load resistor$R_L = 1k\Omega$. On a semi-logarithmic scale the transfer (or $I_{in} - I_{out}$) curve will, therefore, be a straight line. The measured maximum power consumption is 0.5 μW.



(a) (b)

Figure 2.14 DC transfer characteristics of logarithmic circuit

(a) Linear scale (b) Semi-Log scale of x-axis

However, as the bias current was set to 115nA and 170nA, respectively; under the same test conditions, the corresponding output current ranges are about 147.1nA (from -79.4nA to 67.7nA) and 211nA (from -115.2nA to 95.8nA), respectively. It is clear that as the

I_{bias} increased the output dynamic range will increased. Figure (2.15) shows the output current curves with different values of the gain term (I_{bias}).

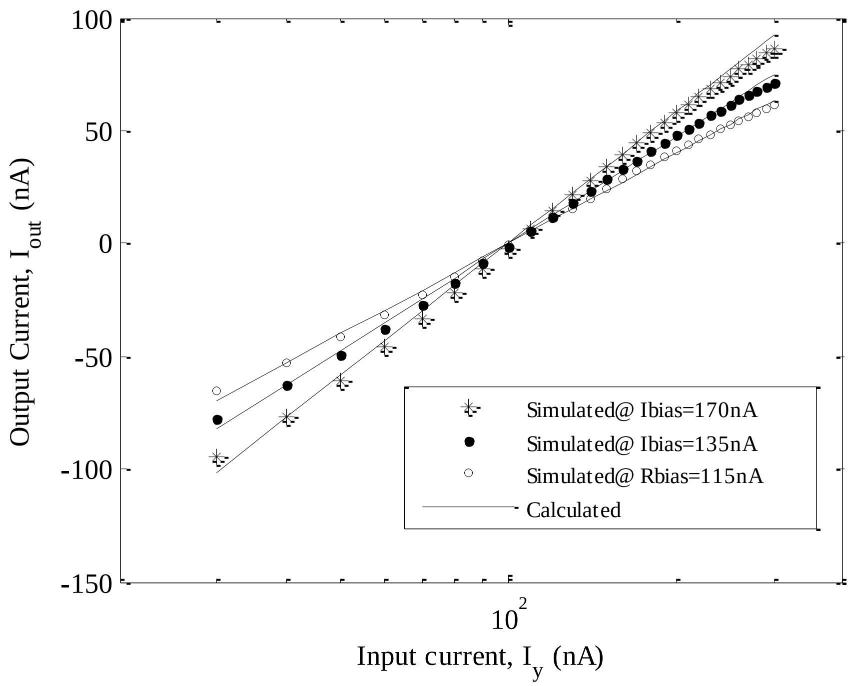


Figure 2.15 The output current with different gain values

If the current I_x is set to 80nA, 100nA and 120nA, the zero output current will be at I_y=80nA, 100nA and 120nA, respectively. The results of the output current with different I_x are shown in figure (2.16). As I_x increased, it is observed that at higher values of the input current,I_y, the corresponding error will be less than the error at lower values of the input current and vice versa. The errors between the simulated results and the theoretical values calculated by equation (2.30) have calculated with I_{bias}=115nA, 135nA and 170nA, respectively. The maximum measured error was 5.7%.

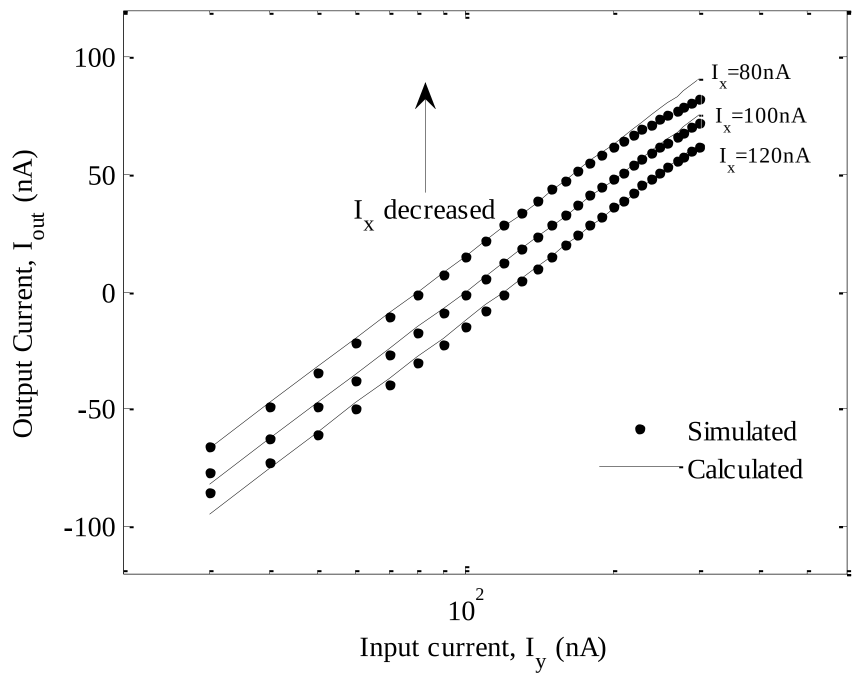


Figure 2.16 the output current with different Ix (different zeros of output current)

The stability of the proposed design against the temperature variation has been confirmed, the temperature was varied from -25 to +75°C (in degree Celsius) and the output current was compared. The output current was normalized to its current at level +25°C and it appears from figure (2.17) that I_{out} shows good performance with temperature variation. The frequency response of the proposed logarithmic circuit is shown in figure (2.18), where the simulation was performed with the I_x=100nA, the magnitude of the input DC and small signals were 165nA and 135nA, respectively, and also a 10pF capacitor was attached to the output as a load. At the bias current I_{bias}=135nA and 115nA, the corresponding −3 dB bandwidth is 7.56 MHz and 7.88 MHz, respectively.

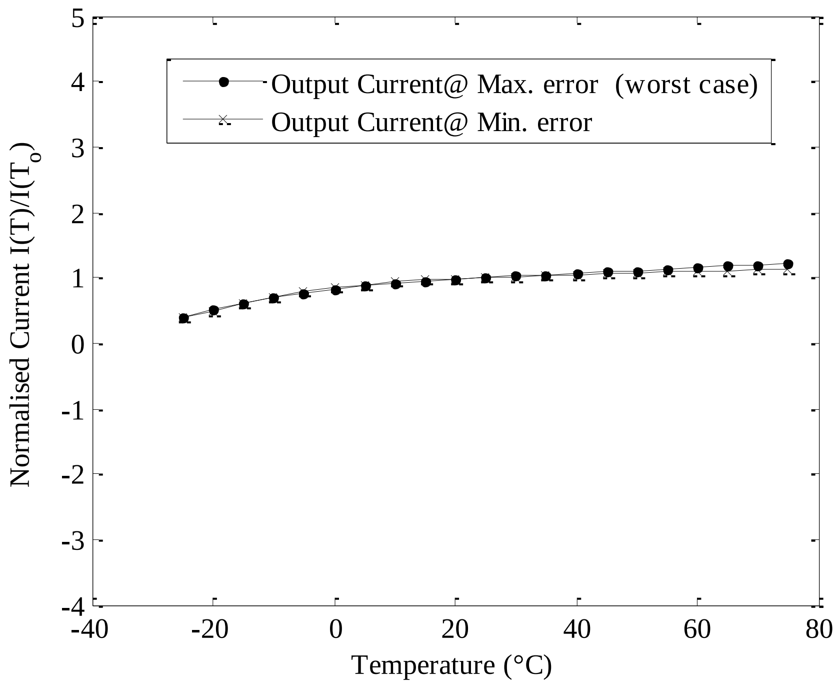


Figure 2.17 Simulation results for temperature independency

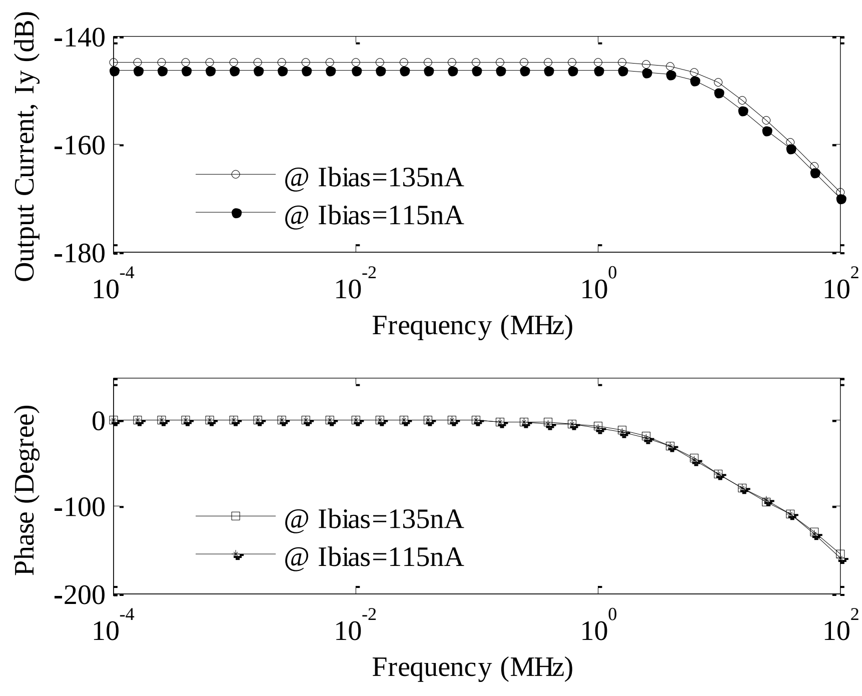


Figure 2.18 Frequency response of the proposed logarithmic circuit

The transient simulation shown in figure (2.19) was measured by applying the sinusoidal input current I_y with peak amplitude of 135nA, DC component of 165nA and the frequency is 1MHz. Figure (2.20) shows the output current waveform for the triangular input signal current of 280nA peak to peak and f=10 kHz. The proposed circuit in figure (2.13) has been simulated for $\log(1/x)$ realization. If I_x varied from 20nA to 350nA (while I_y=100nA) the corresponding output current results in semi-log scale are shown in figure (2.21). The gain of $\log(1/x)$ realization has been adjusted by taking three different values of the bias current, I_{bias}=115nA, 135nA and 170nA, respectively, as shown in Figure (2.22). Figure (2.23) shows the performance of the proposed logarithmic circuit $\frac{I_{bias}}{2} ln\left(\frac{I_y}{I_x}\right)$ for changes of ±1% in the parameter W/L for transistors M5 and M6. Inspection of figure (2.23) shows that the proposed logarithmic function enjoys good performance with variations in W/L with maximum deviation ± 4.5%.

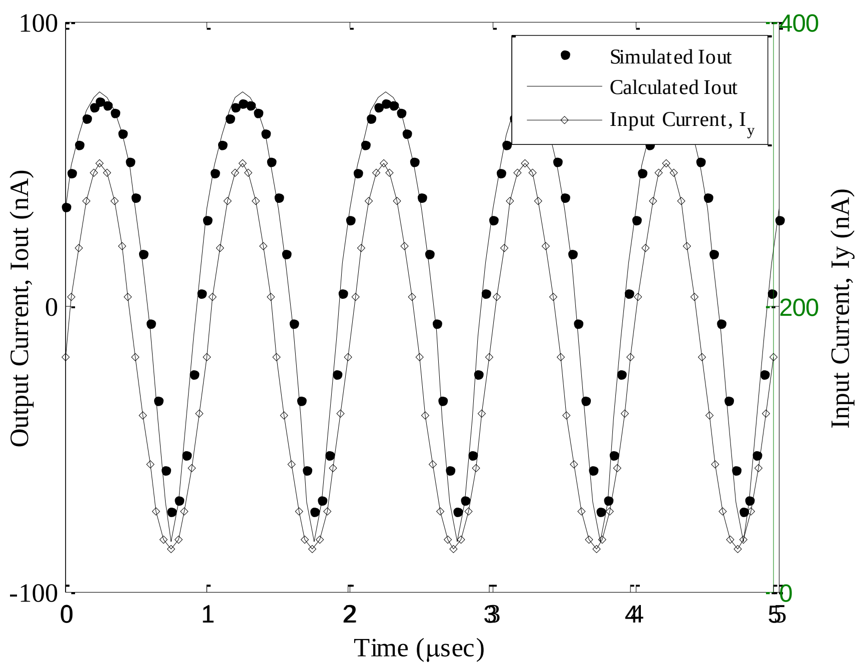


Figure 2.19 Transient response

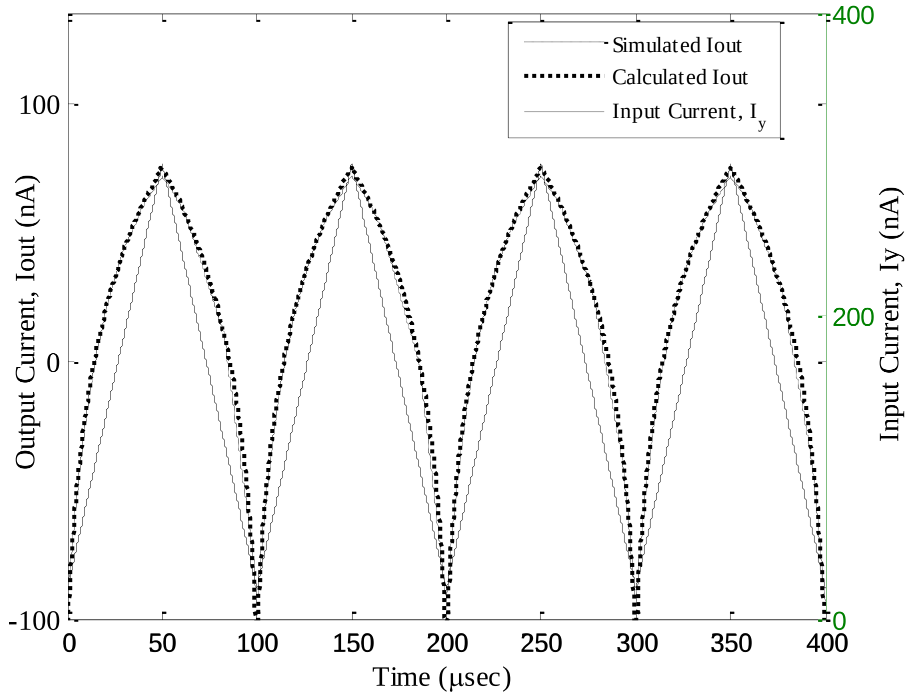


Figure 2.20 Triangular wave response

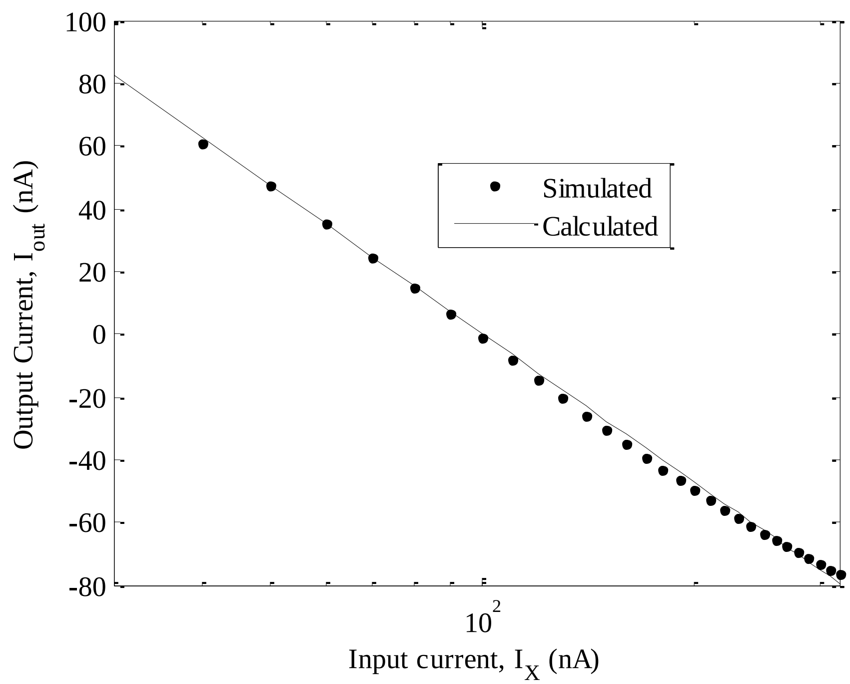


Figure 2.21 The output current response for log(1/x) realization

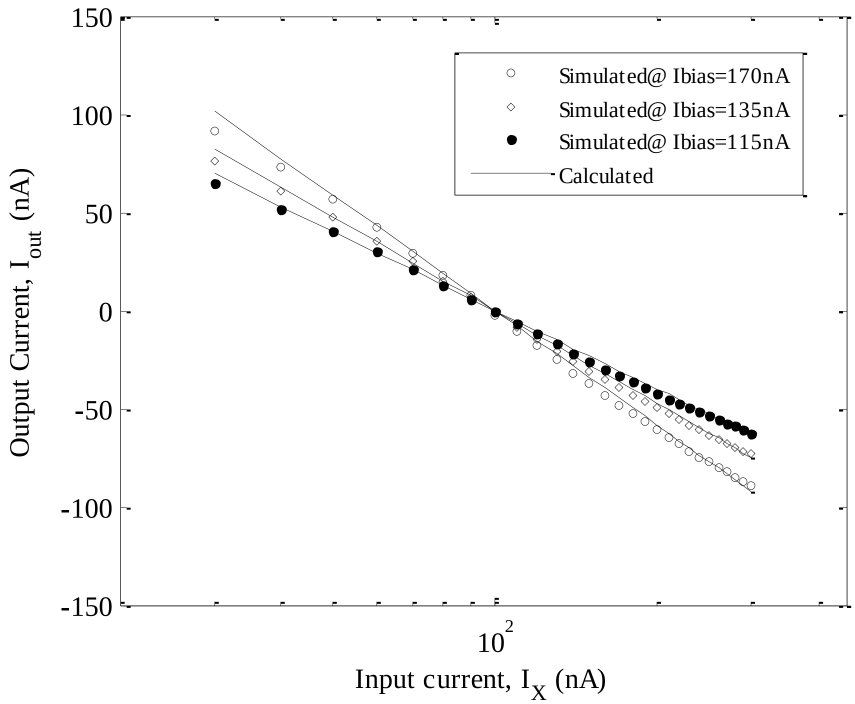


Figure 2.22 Gain adjustment for log(1/x) realization

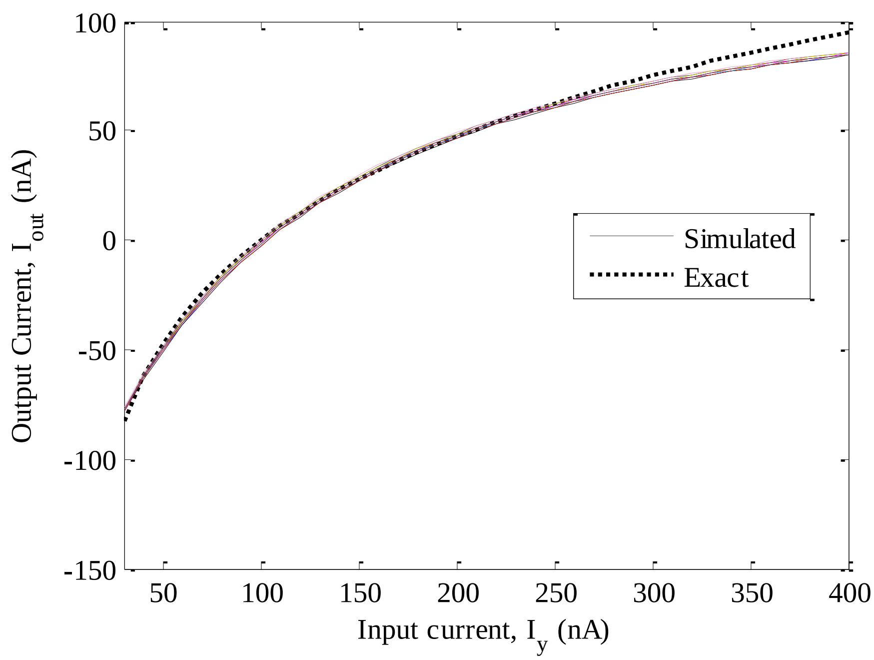


Figure 2.23 Variation of I_{out} with ±1% change in W/L of transistors M5 & M6

The summary of the performance comparison with the most recent published works is listed in table (2.4).

Table 2.4 Performance comparison

Parameter	Performance			
	[26]	**[27]**	**[28]**	**Proposed Work**
Process	0.18µm BiCMOS	0.5µm CMOS	0.18µm CMOS	$0.35\mu m$, 2p4m CMOS
No. of transistors	9 (2 BJT)	21	4	8
Passive elements e.g. R & C	Two resistors	Two resistors	Non	Non
Operation Region	Active (BJT)	Weak inversion	Weak inversion	Weak inversion
Voltage Supply (V)	> 1.3	——	1.8	±0.7
Input\output	Voltage\ voltage	Current\ current	Current\ voltage	Current\current
Max. linearity error	36dB (63%)	NA	5%	4.7%
Power dissipation (µW)	17750	NA	0.3	0.675
Gain controllability	No	Yes	No	Yes
True for $x \geq 1$ $or <$ 1?	Not satisfied	Not satisfied	Satisfied	Satisfied
Temperature	Dependent	Compensated using a PTAT* and resistive cancellation technique	Dependent	Independent

****Proportional-to-absolute- temperature (PTAT)**

2.2 CMOS Exponential Function Circuit

2.2.1 Introduction

The exponential function generator produces an output waveform (current/voltage) which is an exponential function of the input waveform (current/voltage). The exponential characteristics can be easily obtained in BiCMOS or Bipolar technologies using the intrinsic characteristics (I_C/V_{BE}) of the bipolar transistors [38]. Though, it is not easy to realize such function in CMOS technology because the inherent square-law or linear characteristics of MOSFET operating in strong inversion region. So the widely used technique to implement analog exponential function circuits using MOSFET in strong inversion is based on pseudo-approximations. To mathematically implement the exponential function by this method, different approximations have been already introduced; Taylor series 2nd order [39-42], Taylor series 4th order [43], Pseudo exponential [44], Pseudo-Taylor approximation [45], Modified Pseudo-Taylor approximation [46], approximation proposed by Ming-Lang et. al. in 2008 [47].

A MOSFET device biased in weak inversion region is a well-known approach to introduce an exponential function due to the exponential relationship between I_{DS} and V_{GS} of MOSFET in weak inversion regime; see for example references [28-29, 48-49] and some of the references cited therein. Referring to equation (1.3), the drain current of MOSFET in weak inversion region is given by:

$$I_{DS} = 2\mathrm{n}\mu_\mathrm{n}\mathrm{C}_\mathrm{ox}\frac{W}{L}\mathrm{V}_\mathrm{T}^2 e^{\left(\frac{V_{gs}-V_{th}}{nU_T}\right)}$$

Although the low V_{GS} voltage makes this technique efficient in low voltage applications compared with approximations that use MOSFET in strong inversion regime but, obviously, the exponential relation between I_{DS} and V_{GS} is not perfect because it suffers from strongly temperature dependency, threshold voltage variation effect and sensitivity against process variation. Therefore, it is highly preferred to design exponential function generator satisfies the following:

- Accurate and stable exponential function design against temperature variation
- Robust and efficient design versus the supply voltage variation
- Current-input current-output exponential generator thus providing higher frequencies of operation and wider dynamic ranges.
- Extended output range
- Minimum linearity error

In this thesis, a new exponential approximation is proposed. This approximation demonstrates 96 dB output dynamic range over maximum input range $-5.75 \leq x \leq 5.75$ while keeping linearity error in ±0.5dB level. The implemented circuit is designed and simulated using 0.35µm CMOS process.

2.2.2 Proposed Exponential Circuit Design

MOSFETs biased in weak inversion region are used not to utilize the inherent exponential (I_{DS}/V_{GS}) relationship but to simply implement x^2 and x^4 terms using translinear loops. The term x^4 can be easily realized by two cascaded squaring units. Complete design of low voltage (±0.75V) and low power (6.13µW) current-input current-output exponential function generator is presented. A 96 dB range linearly in dB output current with ±0.5 dB linearity error was attained. The output current shows stable characteristics (±1.27dB) with 100℃ temperature range (-25℃ to 75℃). Additionally the design features with low sensitivity against voltage supply variation which is ±3.35dB for ±10% variation from the nominal value.

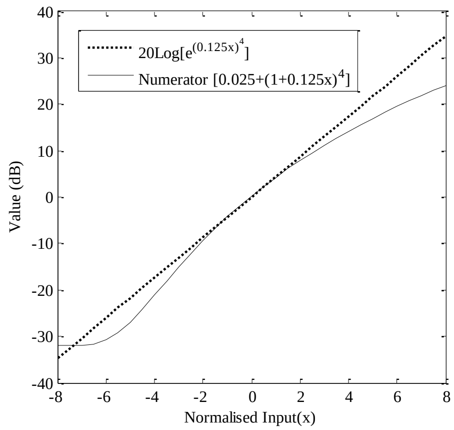
2.2.2.1 The proposed Approach

Motivated by the approximations [39-47], a new approximation formula for exponential function generator is proposed in this thesis as follows:

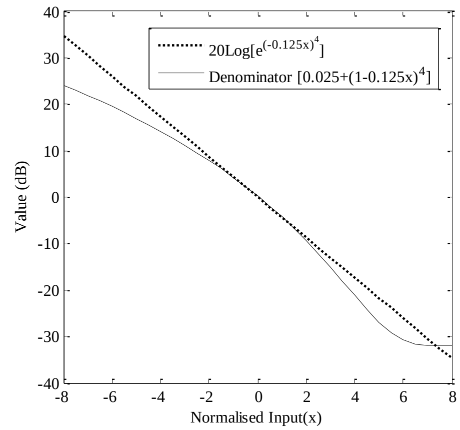
$$e^{x} \cong \frac{0.025+(1+0.125x)^{4}}{0.025+(1-0.125x)^{4}} \qquad (2.45)$$

The plot in dB scale of equation (2.45) is shown in figure (2.24). The dB-value comparison of different approximations described in the prior art and the error of each one with the proposed equation (2.45) are shown in figure (2.25) and figure (2.26), respectively. From figures (2.25) and (2.26), it is evident that the proposed approximation achieves the best output range and maximum normalized input range compared to the other approximations with ±0.5dB error.

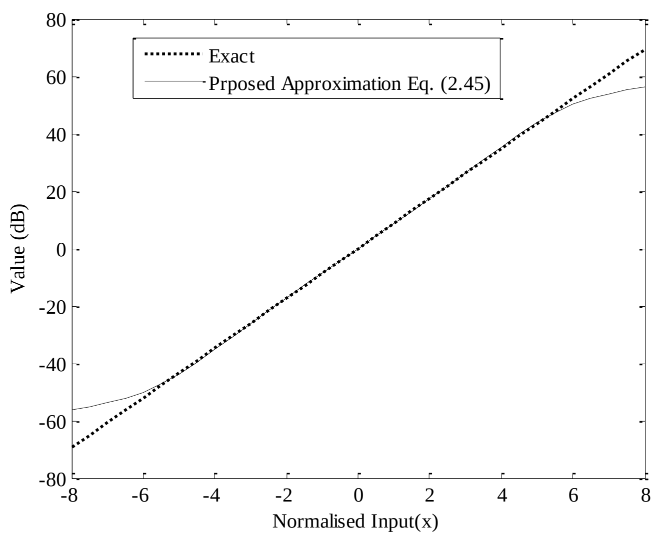
Table (2.5) summarizes the output range and the input range of different approximations compared to the proposed pseudo-exponential in this work with linearity error less than ±0.5dB.



(a)



(b)



(c)

Figure 2.24 Proposed approximation curves (a) Numerator (b) Denominator (c) Proposed equation (2.45)

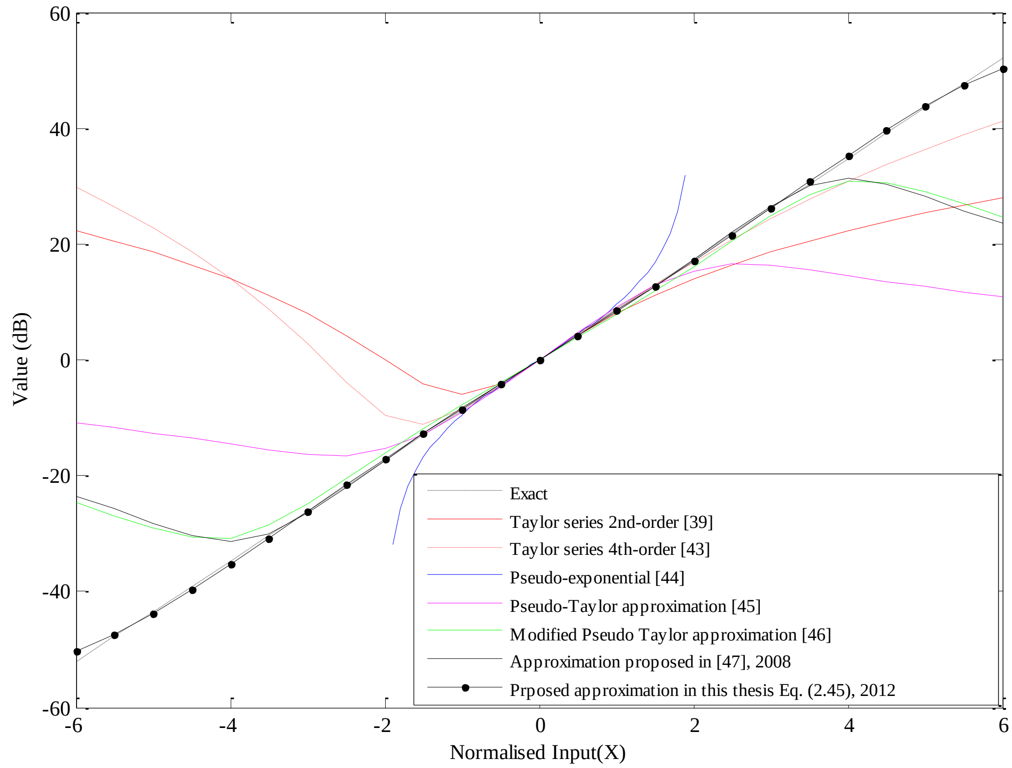


Table 2.25 Different approximations comparison

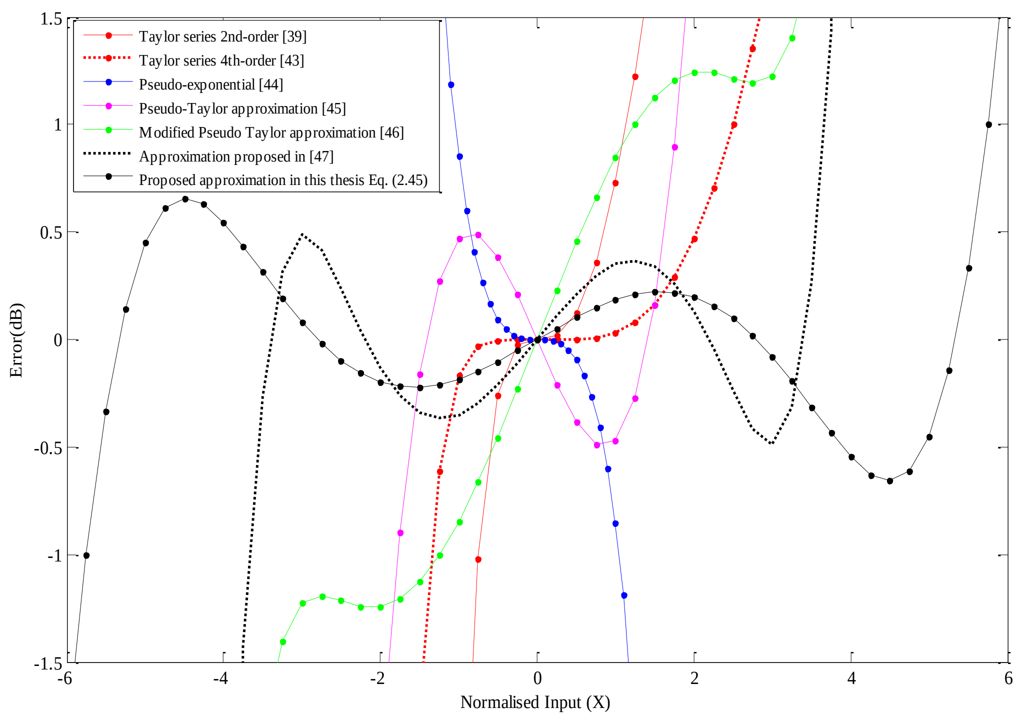


Table 2.26 The error between different approximations and the ideal function

Table 2.5 Different exponential approximations comparison

Approximation	Equation	Input range	Output range
2nd Order Taylor Series [39]	$1 + x + \frac{1}{2}x^2$	$-0.6 \leq x \leq 0.85$	13.3dB
4th Order Taylor Series [43]	$1 + x + \frac{1}{2}x^2 + \frac{1}{3!}x^3 + \frac{1}{4!}x^4$	$-1.2 \leq x \leq 2.0$	30dB
Pseudo exponential [43]	$e^x \cong \frac{1 + 0.5x}{1 - 0.5x}$	$-0.85 \leq x \leq 0.85$	14.8dB
Pseudo-Taylor approximation (m=1) [45]	$e^x = \frac{e^{0.5x}}{e^{-0.5x}} \cong \frac{m + (1 + 0.5x)^2}{m + (1 - 0.5x)^2}$	$-1.08 \leq x \leq 1.08$	17.8dB
Pseudo-Taylor approximation (m=0.82) [45]	$e^x = \frac{e^{0.5x}}{e^{-0.5x}} \cong \frac{m + (1 + 0.5x)^2}{m + (1 - 0.5x)^2}$	$-1.63 \leq x \leq 1.63$	27.2dB
Modified Pseudo-Taylor approximation [46]	$e^x \cong \frac{0.12 + (1 + 0.25x)^2}{0.12 + (1 - 0.25x)^2}$	$-3.1 \leq x \leq 3.1$	56dB
Approximation proposed in 2008 [47]	$e^x = \left[\frac{e^{0.25ax}}{e^{-0.25ax}}\right]^2 \cong \frac{-0.026ax + (1 + 0.25ax)^2}{0.026ax + (1 - 0.25ax)^2}$	$-3.3 \leq x \leq 3.3$	60dB
Proposed	$e^x \cong \frac{0.025 + (1 + 0.125x)^4}{0.025 + (1 - 0.125x)^4}$	$-5.75 \leq x \leq 5.75$	96dB

2.2.2.2 Circuit Description

A. Circuit Design

The full block diagram of the proposed design is shown in figure (2.27). The number of transistors used in the overall circuit is 65 MOSFETs without any passive elements and all of them stacked between ±0.75V voltage-supply.

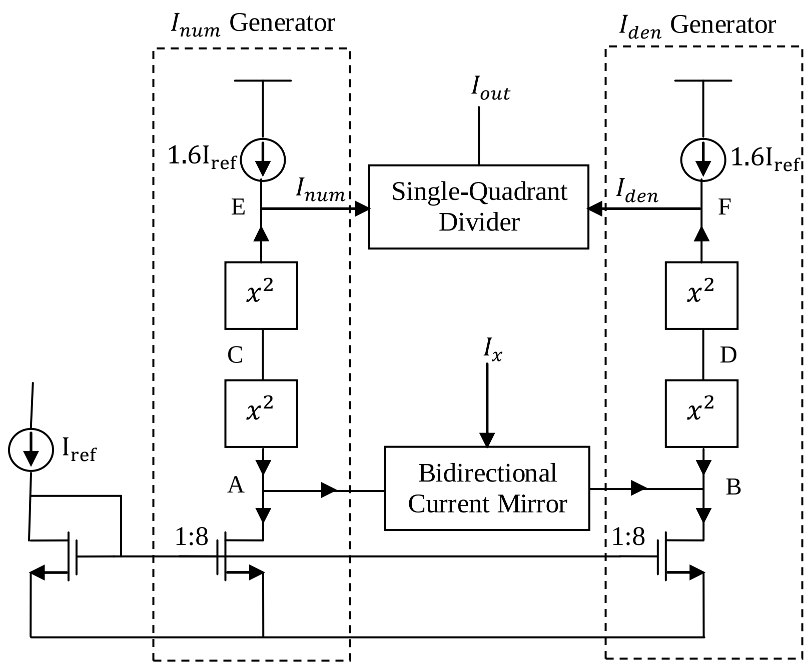


Figure 2.27 Block diagram of the proposed current-mode exponential generator

B. Squaring Unit (SU)

The squaring unit used in block diagram shown in figure (2.27) is shown in figure (2.28). The voltage supply is ±0.75V and the aspect ratios of the transistors are illustrated in table (2.6). The constant currents equal to $4I_{ref}$ and $1.6I_{ref}$ can be easily provided by a proper current source and current sink of current I_{ref}; e.g. if the current I_{ref} in figure (2.27) set to be 25nA, then the constant current $4I_{ref}$ flows through M9 {in squaring unit, figure (2.28)} will be 100nA.

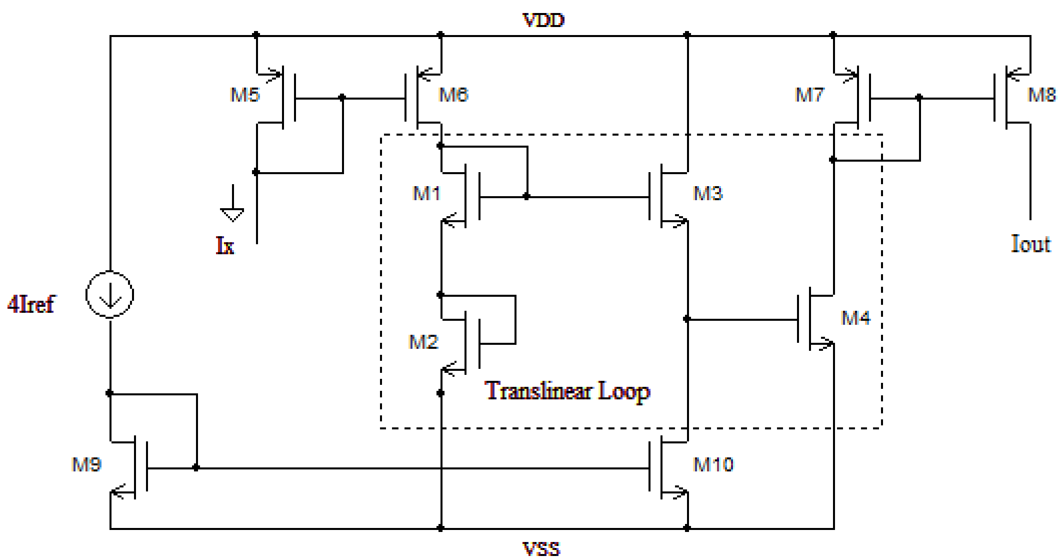


Figure 2.28 Squaring Unit (SU) [17]

With reference to figure (2.28), and by applying Translinear Loop (TL) through M1-M4 transistors then,

$$V_{gs1} + V_{gs2} = V_{gs3} + V_{gs4} \tag{2.46}$$

where V_{gs1}, V_{gs2}, V_{gs3} and V_{gs4} are the gate-to-source voltages of M1, M2, M3 and M4 respectively. From equation (1.3) and equation (2.46), one can easily get the following:

$$I_1 I_2 = I_3 I_4 \tag{2.47}$$

since $I_1 = I_2 = I_x$, $I_3 = 4I_{ref}$ and $I_4 = I_{out}$ then the output current will be expressed as follows:

$$I_{out} = \frac{I_x^2}{4I_{ref}} \tag{2.48}$$

Equation (2.48) represents the current-mode squaring function. Since the squaring circuit is a key block in the proposed current-mode exponential generator as indicated in figure (2.27), the simulation results has been carried out to demonstrate the validity of the theory. The corresponding maximum error is 1.5% and the circuit is stable with temperature variation as demonstrated in figure (2.31).

Table 2.6 Aspect ratios of squaring unit

Transistor	**Aspect Ratio** $\frac{W(\mu m)}{L(\mu m)}$	**Ratio**
M1, M3	$^{3.5}/_{7}$	0.5
M2, M4	$^{91.7}/_{7}$	13.1
M5-M10	$^{7}/_{7}$	1

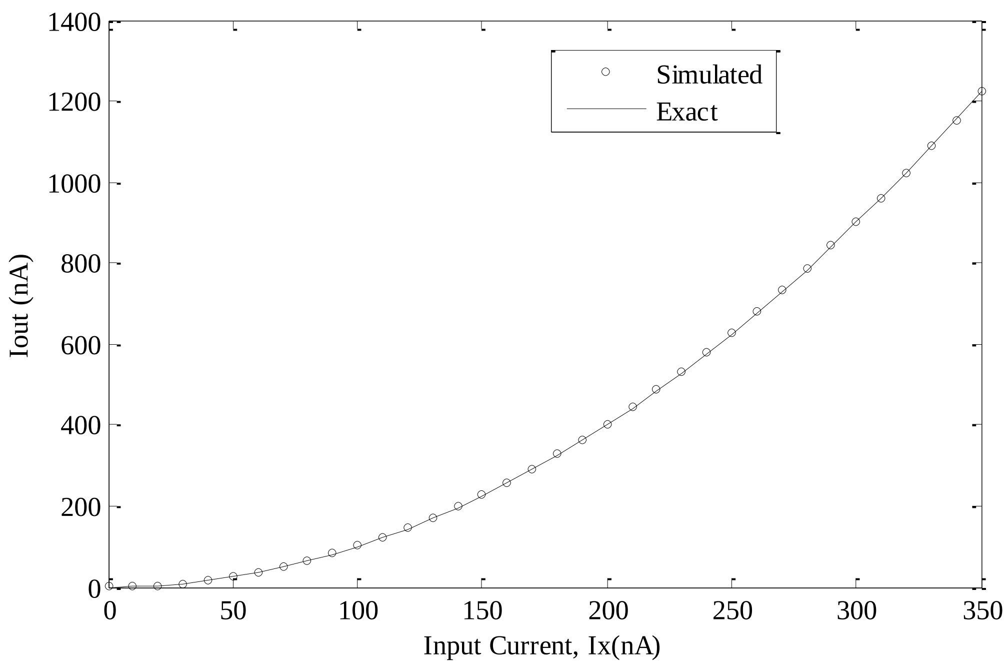


Figure 2.29 Simulation results of the SQ block

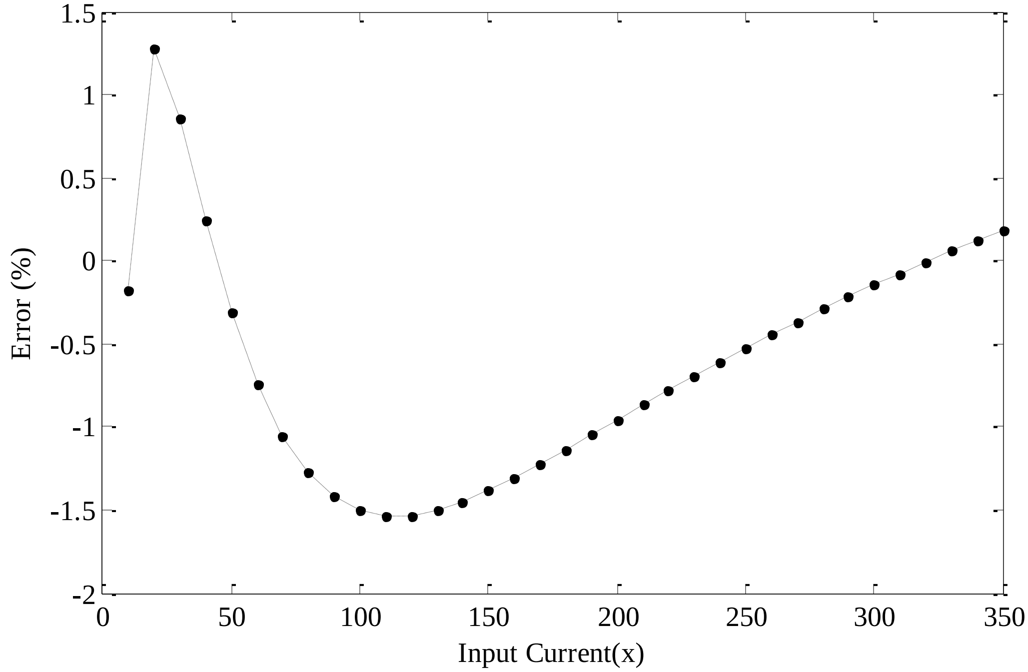


Figure 2.30 Error of the SU block

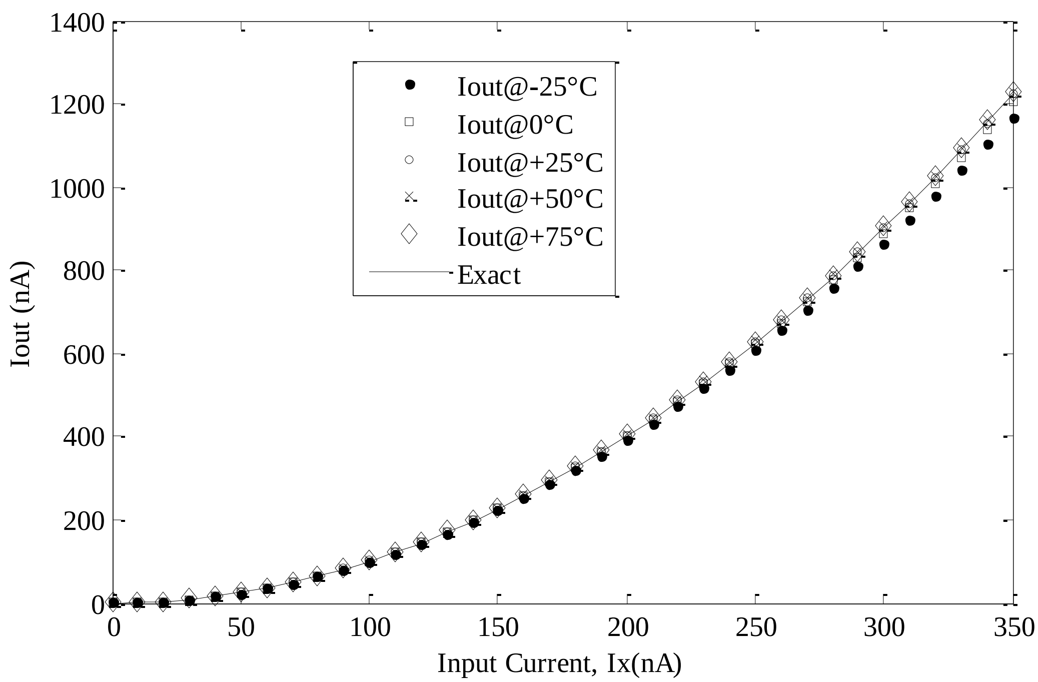


Figure 2.31 SU block results for different Temperatures

C. Current divider

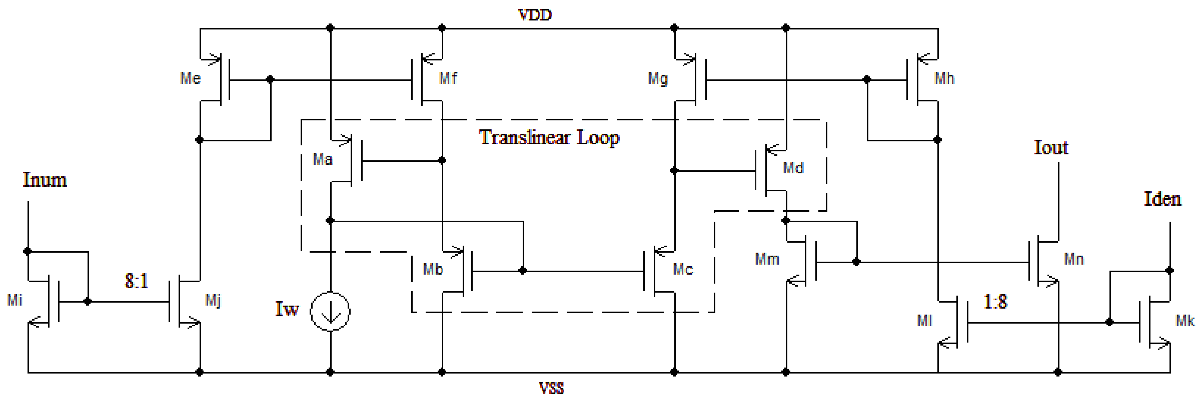


Figure 2.32 Single-Quadrant Divider [50]

The transistors involved in dashed box Ma-Md in figure (2.32) forms a single-quadrant current divider [50] where all transistors are operating in subthreshold region. By analyzing this loop, we will get the following:

$$V_{sga} + V_{sgb} = V_{sgc} + V_{sgd} \tag{2.49}$$

$$I_a I_b = I_c I_d \tag{2.50}$$

with $I_a = I_w$, $I_b = 0.125 I_{num}$, $I_c = 0.125 I_{den}$, and $I_d = I_{out}$. Then the equation (2.50) will be

$$I_{out,Divider} = I_w \frac{I_{num}}{I_{den}} \tag{2.51}$$

The transistor ratios are shown in table (2.7). The $\left(\frac{W}{L}\right)_{j,l} = \frac{1}{8}\left(\frac{W}{L}\right)_{i,k}$ to scale down the currents I_{num} and I_{den} so that transistors Mb (which represents the dividend quantity) and Mc (represents divisor quantity) can absorb this amount of current and as a result the quotient amount (represented by Md) can be improved in terms of accuracy. This implies that the aspect ratios of all the transistors involved in the translinear loop must be selected to meet the anticipated dynamic range of the input and output currents.

Table 2.7 Transistor dimensions of figure 2.2

Transistor	**Aspect Ratio** $\frac{W(\mu m)}{L(\mu m)}$	**Ratio**
Ma, Md	$^{196}/_{1.4}$	140
Mb, Md	$^{175}/_{1.4}$	125
Me-Mh	$^{7}/_{7}$	1
Mi, Mk	$^{19.6}/_{19.6}$	1
Mj, Ml	$^{2.45}/_{19.6}$	0.125
Mm-Mn	$^{1}/_{1}$	1

D. Current Mirror (CM):

Figure (2.33) shows the current mirror with two output currents. If the input current is I_x then two copies of this current can obtained at the output, I_x and $-I_x$. The dimensions of CM are listed in table (2.8). The simulation results with ±0.75V voltage supply are shown to verify the functionality of the circuit. Figure (2.34) and figure (2.35) shows the DC transfer characteristics and transient response, respectively. The error calculated is very small as shown in figure (2.36).

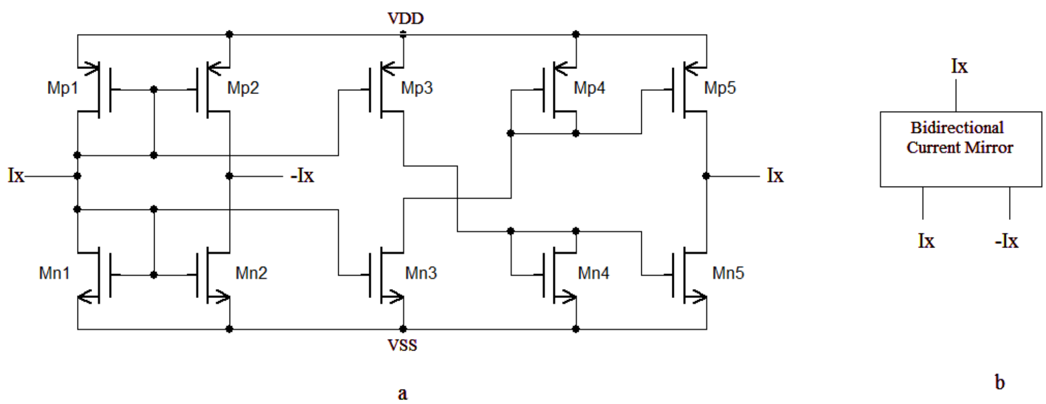


Figure 2.33 current mirror (a) circuit (b) symbol

Table 2.8 Dimensions of CM (figure 2.33)

Transistor	Aspect Ratio $\frac{W(\mu m)}{L(\mu m)}$	Ratio
Mn1- Mn5	$^{1}/_{10}$	0.1
Mp1-Mp5	$^{1.7}/_{10}$	0.17

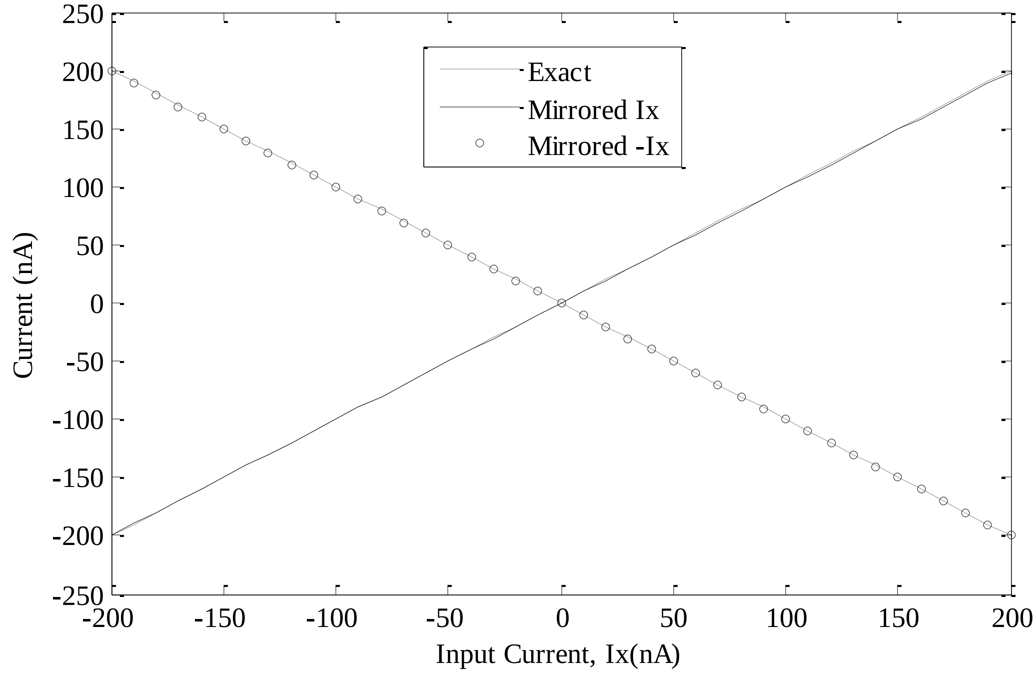


Figure (2.34) DC curves of BDCM

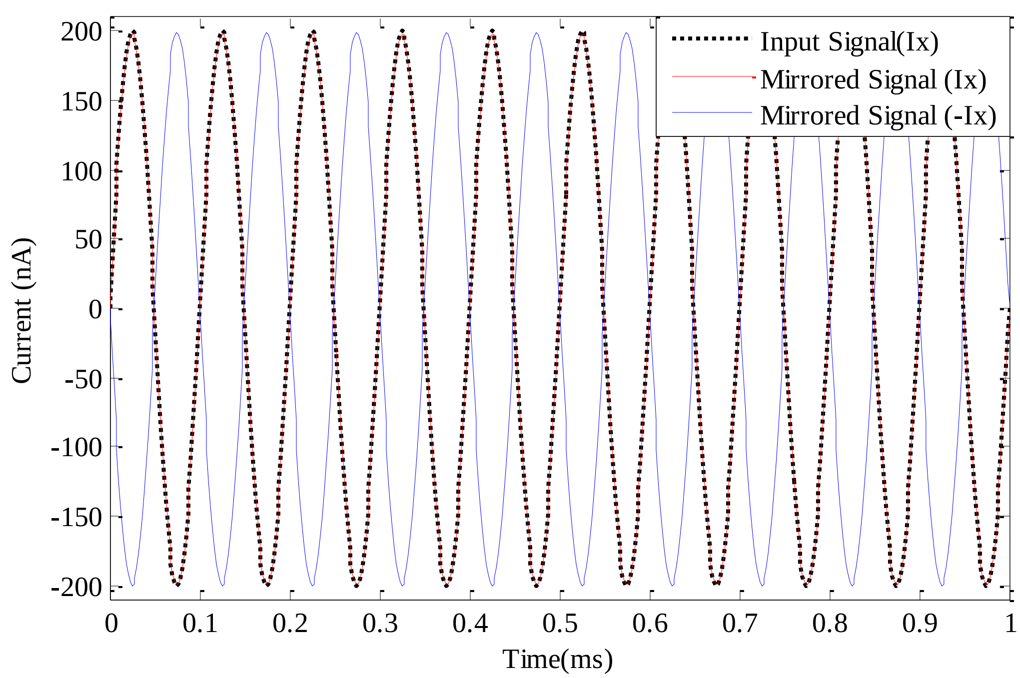


Figure 2.35 Transient response of BDCM

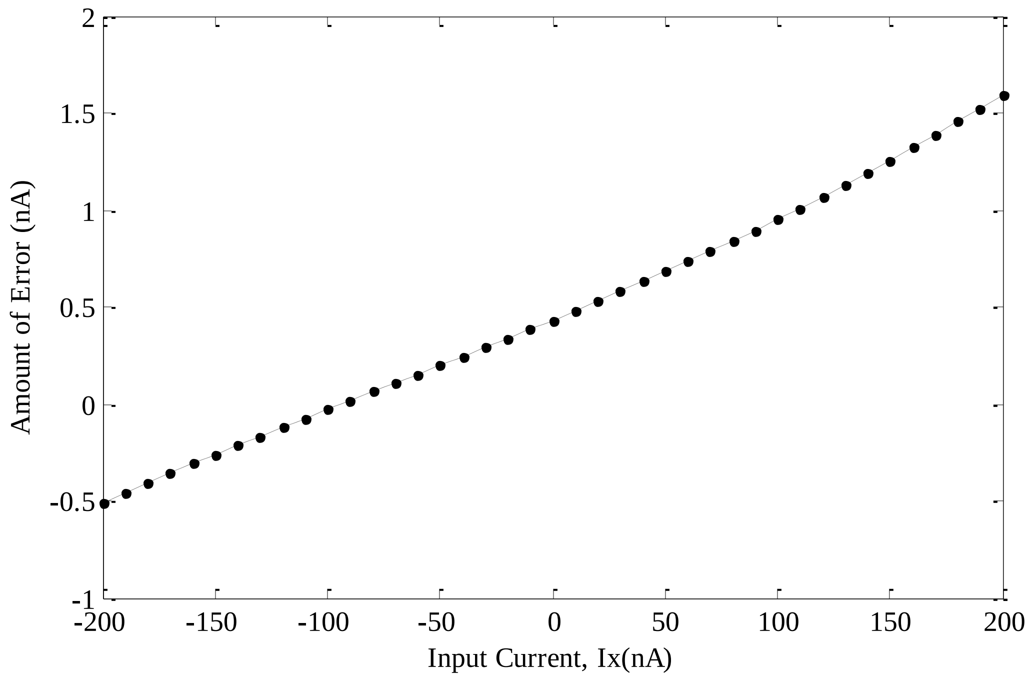


Figure 2.36 Amount of Error (nA) for BDCM

With the reference to the figure (2.27) there are six nodes A, B, C, D, E and F. The current flows through these nodes as follows:

$$I_A = 8I_{ref} + I_x = 8I_{ref}\left(1 + 0.125\frac{I_x}{I_{ref}}\right) \tag{2.52}$$

$$I_B = 8I_{ref} - I_x = 8I_{ref}\left(1 - 0.125\frac{I_x}{I_{ref}}\right) \tag{2.53}$$

$$I_C = \frac{\left(8I_{ref}\right)^2\left(1+0.125\frac{I_x}{I_{ref}}\right)^2}{4I_{ref}} \tag{2.54}$$

$$I_D = \frac{\left(8I_{ref}\right)^2\left(1-0.125\frac{I_x}{I_{ref}}\right)^2}{4I_{ref}} \tag{2.55}$$

$$I_E = \frac{(8I_{ref})^4\left(1+0.125\frac{I_x}{I_{ref}}\right)^4}{(4I_{ref})^3} = 64I_{ref}\left(1+0.125\frac{I_x}{I_{ref}}\right)^4 \tag{2.56}$$

$$I_F = \frac{(8I_{ref})^4\left(1-0.125\frac{I_x}{I_{ref}}\right)^4}{(4I_{ref})^3} = 64I_{ref}\left(1-0.125\frac{I_x}{I_{ref}}\right)^4 \tag{2.57}$$

$$I_{num} = 1.6I_{ref} + 64I_{ref}\left(1+0.125\frac{I_x}{I_{ref}}\right)^4 = 64I_{ref}\left[0.025+\left(1+0.125\frac{I_x}{I_{ref}}\right)^4\right] \tag{2.58}$$

$$I_{den} = 1.6I_{ref} + 64I_{ref}\left(1-0.125\frac{I_x}{I_{ref}}\right)^4 = 64I_{ref}\left[0.025+\left(1-0.125\frac{I_x}{I_{ref}}\right)^4\right] \tag{2.59}$$

By recall equation (2.51), the output current of the proposed EXPFG will be

$$I_{out} = I_w\frac{I_{num}}{I_{den}} = I_w\left\{\frac{\left[0.025+\left(1+0.125\frac{I_x}{I_{ref}}\right)^4\right]}{\left[0.025+\left(1-0.125\frac{I_x}{I_{ref}}\right)^4\right]}\right\} \cong I_w e^{\left(\frac{I_x}{I_{ref}}\right)} \tag{2.60}$$

$$I_{out} = I_w e^{\left(\frac{I_x}{I_{ref}}\right)} \tag{2.61}$$

where I_{out} is the output current, I_x is the input ac signal, I_{ref} is a constant current and I_w is a DC component which can be used to scale the output signal. From equation (2.61), it is clear that the exponential current-mode generator can be realized and its output current can be adjusted by I_w. The full circuit of the proposed current-mode exponential function generator (EXPFG) is shown in figure (2.37).

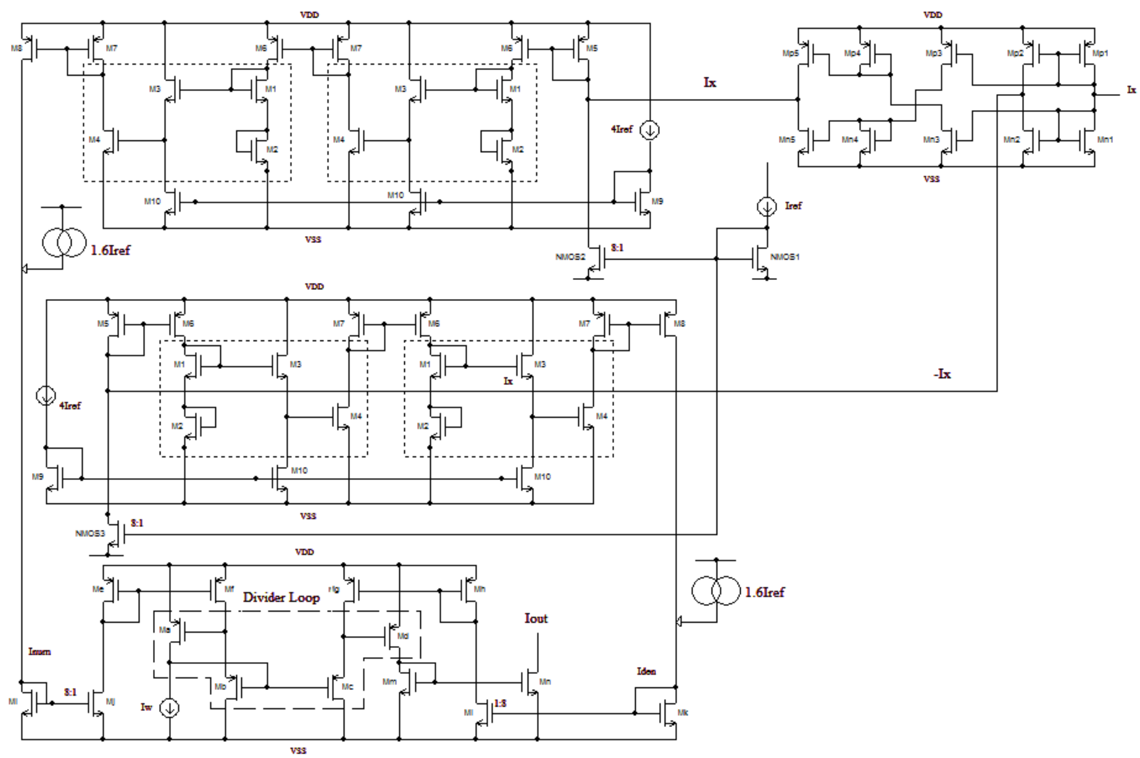


Figure 2.37 The full circuit of the exponential function

2.2.2.3 Current Mirror Mismatch

Referring to the figure (2.27), if the current mirror $1.6I_{ref}$ is not exact (i.e. it is equal to $1.6I_{ref} + \Delta I_{ref}$), then equations (2.58) to (2.60) can be reevaluated and the output current will be expressed as (See appendix A for more details):

$$I_{out} = I_w \frac{I_{num}}{I_{den}} = I_w \left\{ \frac{\left[k + \left(1 + 0.125 \frac{I_x}{I_{ref}} \right)^4 \right]}{\left[k + \left(1 - 0.125 \frac{I_x}{I_{ref}} \right)^4 \right]} \right\} \tag{2.62}$$

where $k = 0.025 + \frac{\Delta I_{ref}}{64 I_{ref}}$. Assume that there is ±10% deviation from the exact value (0.025); the results shown in figure (2.38) show that the deviation is not significant.

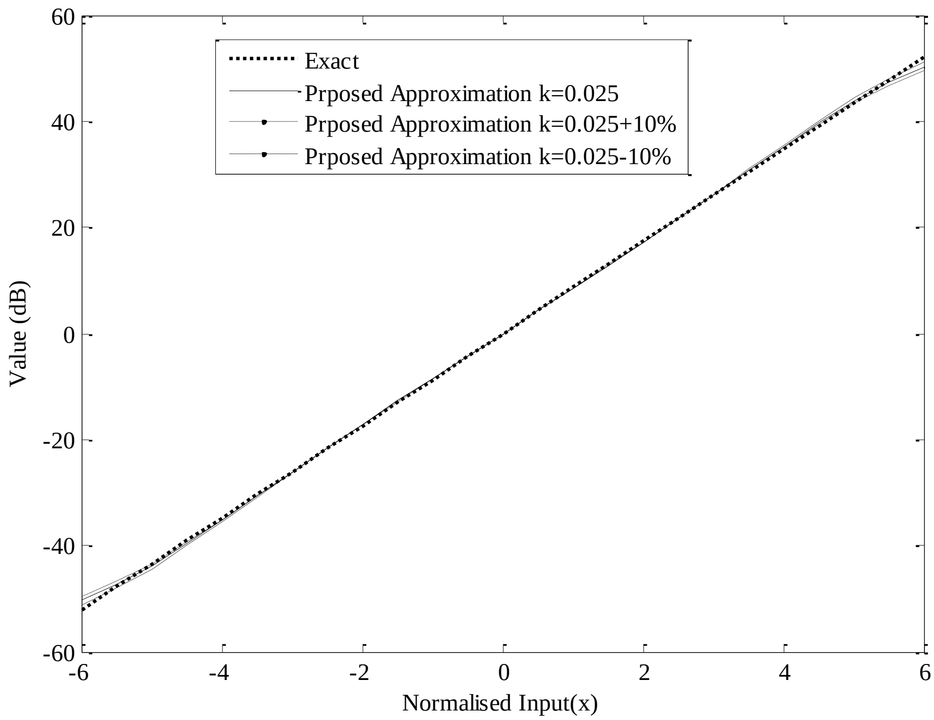


Figure 2.38 Effect of mismatch in the current mirror

2.2.3 Simulation Results

The circuit in figure (2.37) is used to implement the proposed function and is verified by simulation in 0.35μm CMOS process technology with supply voltage ±0.75V. The threshold voltage of PMOS and NMOS is 0.833V and 0.572V in this process technology. The Tanner simulation result is illustrated in figure (2.39) where I_{ref} equals to 25nA. Thus the x-axis, $150nA \leq I_x \leq 150nA$, can be normalized as -6≤ x ≤6 for comparing to figure (2.25). The curve of the proposed function is very close to the ideal exponential function, $I_w e^{\left(\frac{I_x}{25nA}\right)}$, with a high output dynamic range, nearly 96dB. The error between the proposed function and the ideal exponential function, $I_w e^{\left(\frac{I_x}{25nA}\right)}$, is limited to ±0.5dB when $-137.5nA \leq I_x \leq 137.5nA$, as illustrated in figure (2.40).

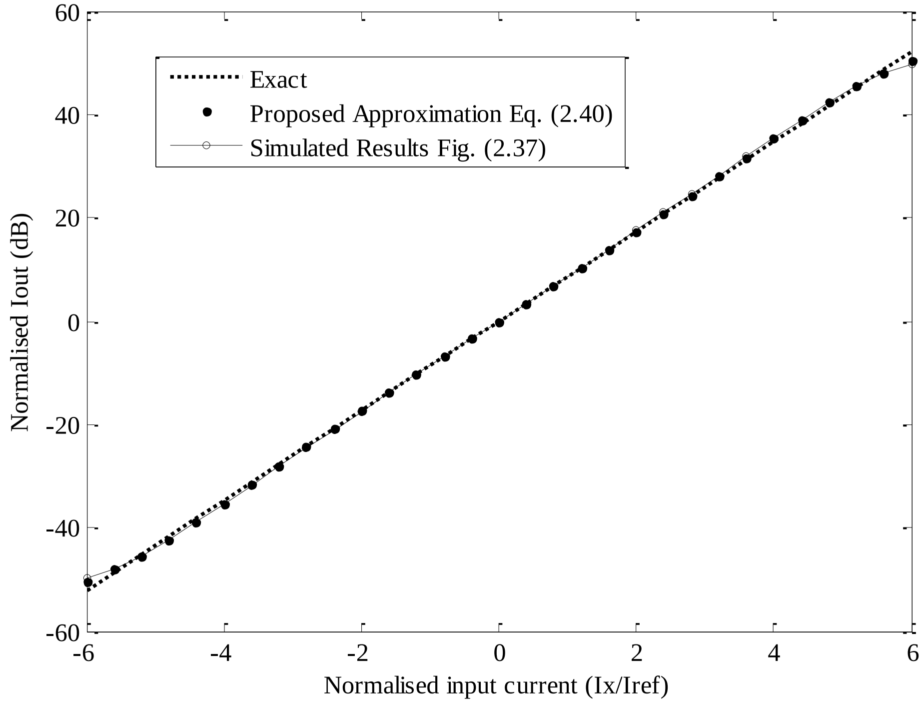


Figure 2.39 Linear-in-dB characteristics of the proposed EXPFG

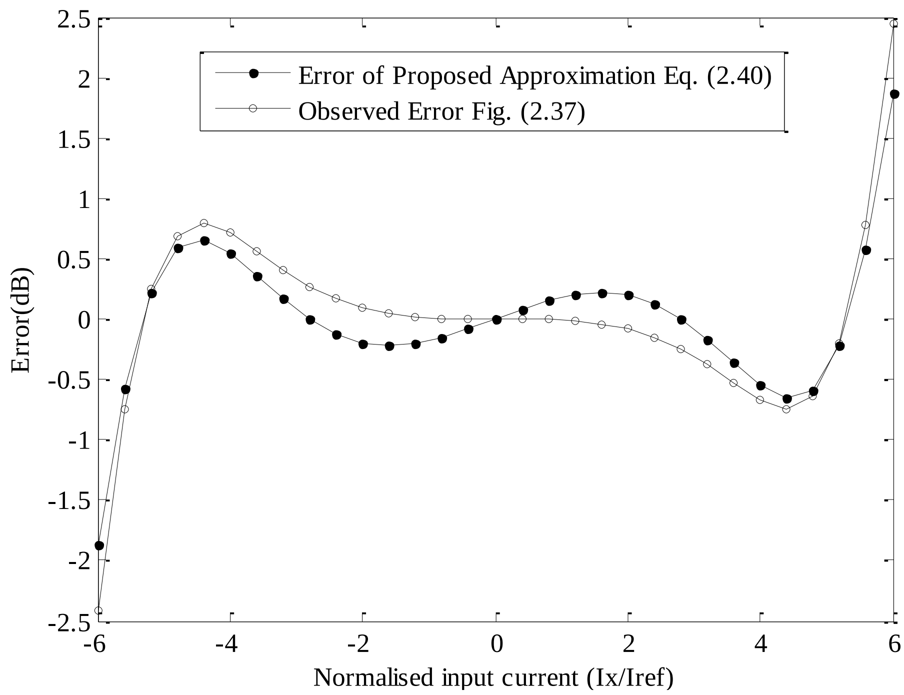


Figure 2.40 The error in dB between the equation (2.45) and its CMOS implementation figure (2.37)

The simulation of transient response has been carried out with sinusoidal input signal of frequency 5 kHz. The results are shown in figure (2.41). Figure (2.42) presents the results of normalized output current I_{out} (dB) at -25℃, +25℃ and +75℃. As expected the input\output characteristics are roughly stable with temperature variation. The linearity error remains less than ±1.5dB for the full scale of the input current range. The maximum deviation of the output current was about ±1.27 dB and is occurred for the normalized value $\frac{I_x}{I_{ref}} = 5.25$.

Figure (2.43) clarifies the results of the normalized output current I_{out} (dB) characteristics for ±10% variation of the supply voltages V_{DD} and V_{SS} at the nominal temperature of 25°C. The corner values of the supply voltage were ±0.675 V and ±0.825 V, where ±0.75 V was the nominal supply. Table (2.9) summarizes the performance of the proposed circuit with recently published works.

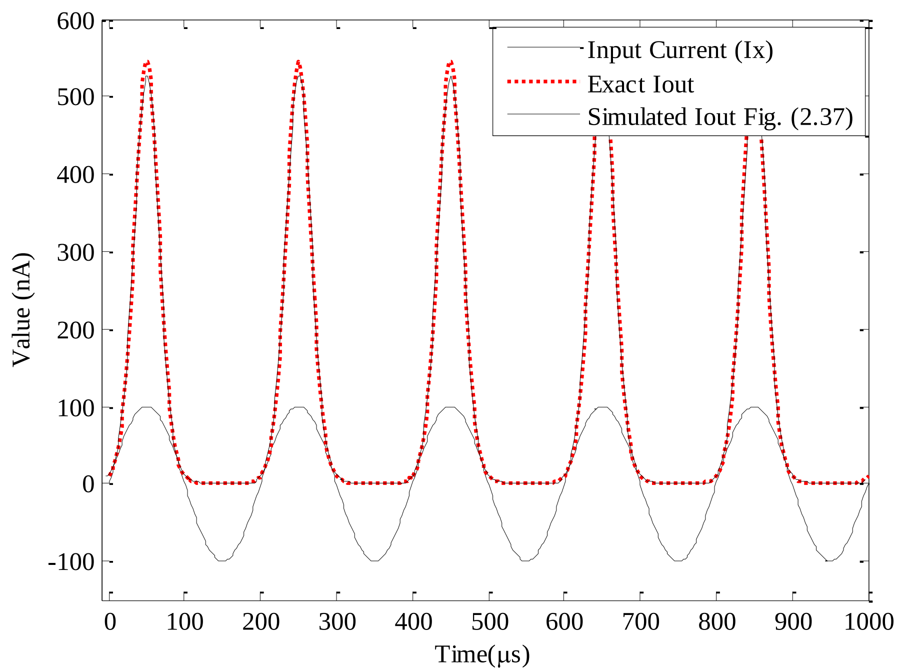


Figure 2.41 Transient response

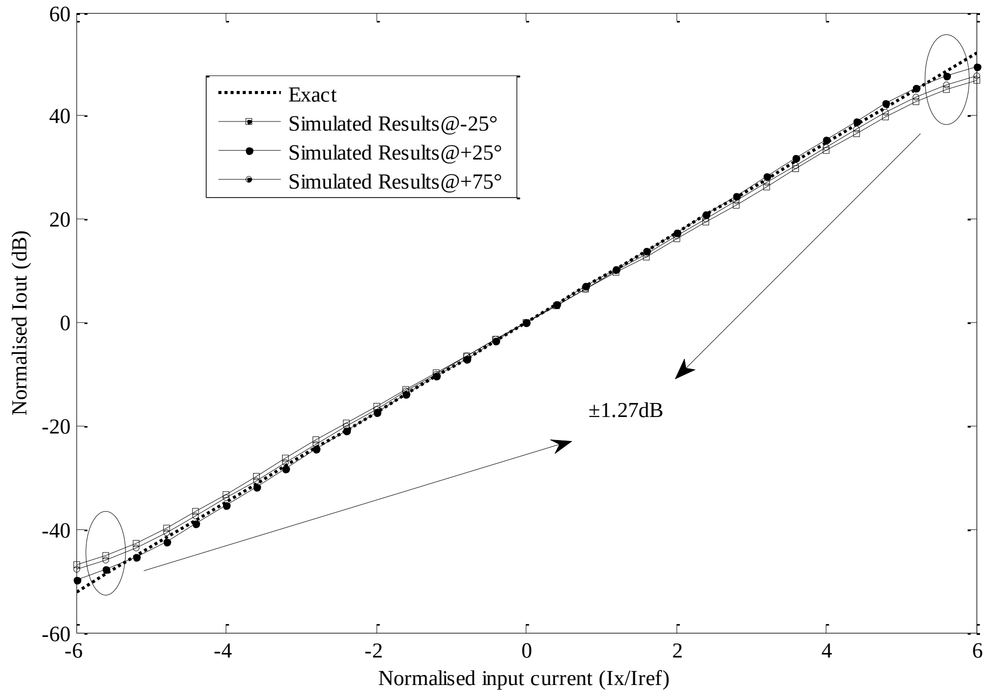


Figure 2.42 Temperature variation -25℃, +25℃ and +75℃

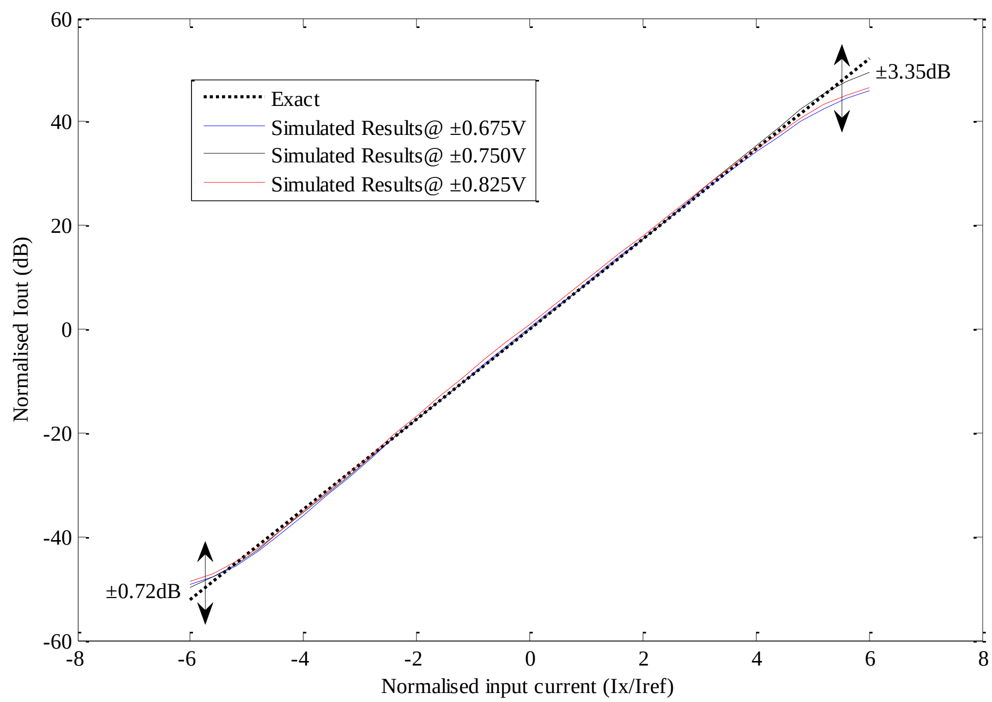


Figure 2.43 Linear-in-dB characteristics for ±10% variation in voltage supply

Table 2.9 Performance comparison table between different exponential function circuits

Parameter	[28]	[39]{1}	[47]	[49]	This work
Year	2011	2005	2008	2012	2012
Voltage Supply	1.8V	1V	1.8V	1.5V	±0.75V
Process	0.18µm CMOS	0.35µm CMOS	0.18µm CMOS	0.35 µm CMOS	0.35 µm, 2p4m CMOS
Power dissipation	214nW	3.5µW	NA	400uA	6.13uW
Technique	Exact	Approximation	Approximation	Exact	Approximation
Operation Region	Weak inversion	Weak inversion	Strong inversion	Weak inversion	Weak inversion
Input Signal	voltage	current	current	voltage	current
Output Signal	current	current	current	current	current
Linear-in-dB range	NA	8.5dB	58dB	40dB	96dB
Linearity error	±0.92dB	±0.45dB	±0.5dB	±0.75dB	±0.5dB
BW	NA	NA	NA	NA	105kHz
ΔT range	Dependent	NA	NA	-10℃ : 70℃	-25℃ : 75℃
Error due ΔT	Dependent	NA	NA	±3dB	±1.27dB
ΔV range	NA	NA	NA	±10% V	±10% V
Error due ΔV	NA	NA	NA	±1dB	±3.35dB

{1} Experimental

CHAPTER 3

VARIABLE GAIN AMPLIFIERS (VGAs)

To verify the effectiveness of the logarithmic and exponential structures proposed in chapter 2, different log-antilog based circuits for different applications have been developed in chapters 3 & 4. In this chapter two kinds of variable-gain amplifiers are presented; logarithmically-controlled variable-gain attenuator (LCVGA) and exponential-control variable-gain amplifier. Variable-gain amplifier can be used in many applications that need gain control to improve the performance of the overall system.

3.1 Logarithmically-Controlled Variable-Gain Attenuator (LCVGA)

This design presents a novel current-mode building block for analog signal processing, namely logarithmic-control variable-gain attenuator (LCVGA). It consists of two Operational Transconductance Amplifier (OTA) and two PMOS transistors designed to work in subthreshold regime. The circuit operates from ±0.75V DC power supply with three transistors stacked in the electric path between +ve supply and –ve supply and consumes 0.6 µW. The output range is 43 dB with maximum error less than ±0.5dB. The functionality of the proposed design was confirmed using Tanner tool in 0.35µm CMOS process technology. This circuit is expected to be a useful building block for AGCs for Bionic Ears (BE).

3.1.1 General Overview

In signal processing, sometimes the signal may be too large to be handled. So compression (i.e. attenuation) process is needed to scale down the signal in order to process it properly. Such block can be found in high frequency applications like RF receivers [51], low frequency applications e.g. analog bionic ear processor [52] and automated gain control (AGCs) in auditory prostheses [53]. The attenuation characteristics can be carried out by a linear function, power-law compression or logarithmic characteristics. The inherent characteristics of MOSFET in subthreshold region have been utilized to introduce a current-mode logarithmically-controlled variable-gain attenuator suitable for low power AGCs.

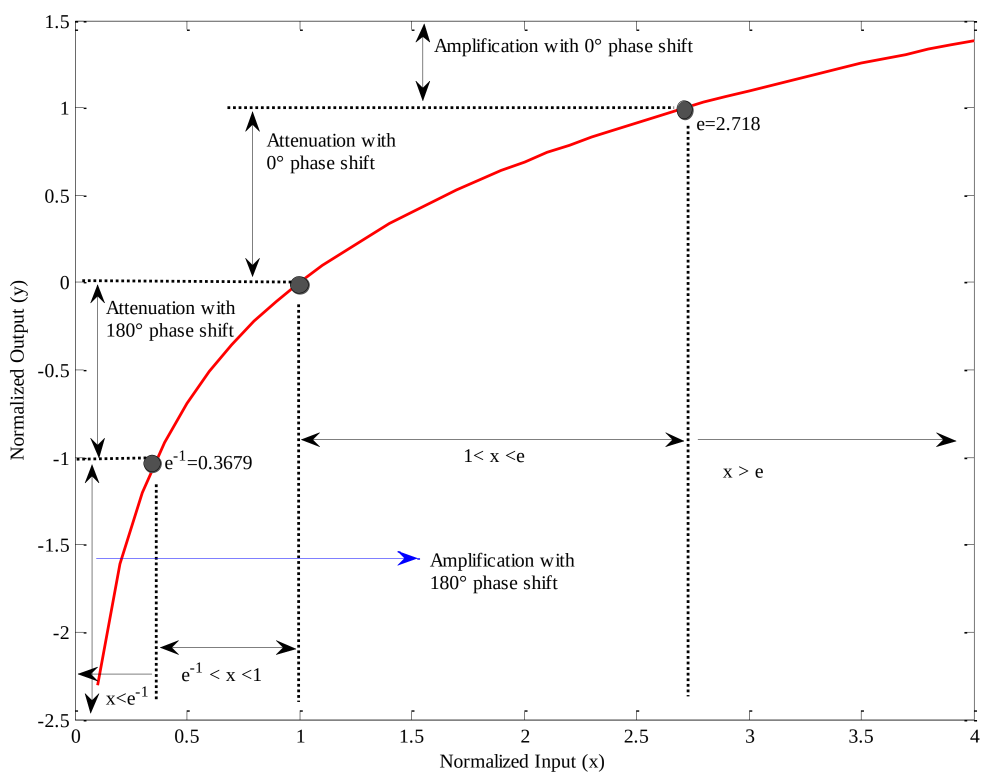


Figure 3.1 Characteristics of the natural logarithmic curve

To more clarify the different regions of natural logarithmic input/output transfer curve; see figure (3.1). It can be seen that the compression (attenuation) process happened as follows:

$$Attenuation\ when \begin{cases} 1 < x < e & 0℃\ phase\ shift \\ e^{-1} < x < 1 & 180℃\ phase\ shift \end{cases}$$

3.1.2 Proposed LCVGA

The complete circuit diagram of the proposed design is shown in figure (3.2). It consists of two OTAs, current mirror and two PMOS transistors biased in weak inversion region used for current- to-voltage compression. Transistors in dashed boxes (M1-M4 and M7-M10) form OTA_1 and OTA_2 respectively. Transistors M11, M12& M13 form the current mirror required to mirror I_{bias} from M11 into transistor M12 and M13 with 1:1 ratio. Figure (3.3) shows the block diagram for the realization of the proposed function.

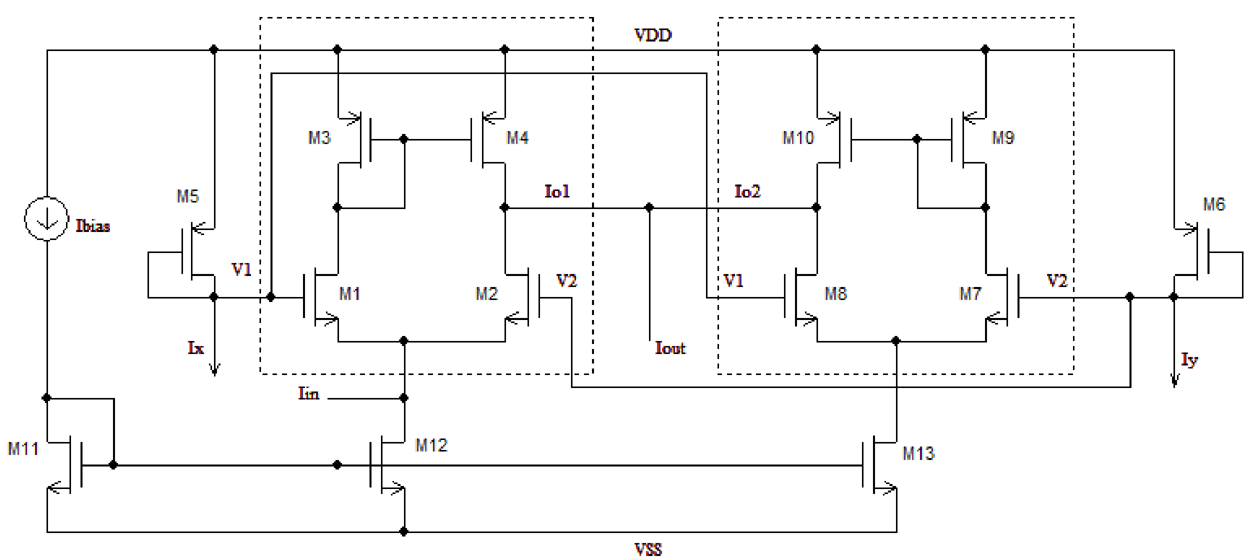


Figure 3.2 Proposed LCVGA

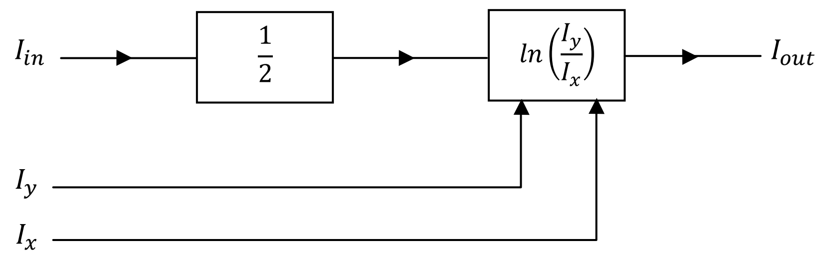


Figure 3.3 Block diagram for the realization of figure (3.2)

With reference to figure (3.2), the output current of the OTA is given by:

$$I_{out(OTA)} = g_m(V_1 - V_2) \tag{3.1}$$

The transconductance g_m of the transistor in weak inversion region is given by:

$$g_m = \frac{I_D}{nU_T} \tag{3.2}$$

Where $g_m = \frac{I_D}{nU_T}$, the transconductance of MOS in weak inversion used in the OTAs, I_D is the drain current of MOSFETs form differential pairs in OTA1 and OTA2 and is given by $I_D = \frac{I_{bias}}{2}$, V_1 and V_2 are the two input voltages. The control current I_x and input current I_y are converted to voltages V_1 and V_2 in logarithmic form through transistors M_5 and M_6 respectively according to the following equations:

$$V_1 = V_{DD} - V_{sg5} = V_{DD} - nU_T \ln\left(\frac{I_x}{I_{Do}}\right) - V_{th} \tag{3.3}$$

$$V_2 = V_{DD} - V_{sg6} = V_{DD} - nU_T \ln\left(\frac{I_y}{I_{Do}}\right) - V_{th} \tag{3.4}$$

Where V_{DD} is the supply voltage and V_{sg} is the source to gate voltage, $U_T = \frac{KT}{q}$ is the thermal voltage, n is the slope factor and I_{Do} is the leakage current of the MOSFET.

Combining equations (3.3) and (3.4) yields

$$(\mathrm{V_1} - \mathrm{V_2}) = \mathrm{nU_T} \ln\left(\frac{\mathrm{I_y}}{\mathrm{I_x}}\right) \tag{3.5}$$

$$(\mathrm{V_2} - \mathrm{V_1}) = \mathrm{nU_T} \ln\left(\frac{\mathrm{I_x}}{\mathrm{I_y}}\right) \tag{3.6}$$

According to equation (3.1) and by combining equations (3.2)-(3.6), one can easily get the equations (3.7)-(3.10)

$$I_{O1} = g_m(V_1 - V_2) \tag{3.7}$$

$$I_{O2} = g_m(V_2 - V_1) \tag{3.8}$$

$$I_{O1} = g_m \mathrm{nU_T} \ln\left(\frac{\mathrm{I_y}}{\mathrm{I_x}}\right) \tag{3.9}$$

$$I_{O2} = g_m \mathrm{nU_T} \ln\left(\frac{\mathrm{I_x}}{\mathrm{I_y}}\right) = -g_m \mathrm{nU_T} \ln\left(\frac{\mathrm{I_y}}{\mathrm{I_x}}\right) \tag{3.10}$$

It is easy to show that the output currents of OTA1 and OTA2 are given by equations (3.11) and (3.12) expressed by:

$$I_{O1} = \left(\frac{I_{in}+I_{bias}}{2}\right) \cdot \ln\left(\frac{I_y}{I_x}\right) \tag{3.11}$$

$$I_{O2} = -\frac{I_{bias}}{2} \cdot \ln\left(\frac{I_y}{I_x}\right) \tag{3.12}$$

With reference to figure (3.1) and from equations (4) and (5) the output current is given by:

$$I_{out} = I_{O1} + I_{O2}$$

$$I_{out} = \frac{I_{in}}{2} \ln\left(\frac{I_y}{I_x}\right) \tag{3.13}$$

The amplifier current gain is given by:

$$A_i = \frac{I_{out}}{I_{in}} = \frac{1}{2} \ln\left(\frac{I_y}{I_x}\right)$$

$$\mathrm{A_i} = \ln\left(\frac{I_y}{I_x}\right)^{\frac{1}{2}} \tag{3.14}$$

According to equation (3.14) a current-mode variable-gain attenuator can be realized and its attenuation amount can be logarithmically controlled by the controlled currents I_y and I_x. The output signal can be attenuated twice, one by the square-root and then by the natural logarithmic characteristics.

3.1.3 Simulation Results

The proposed LCVGA was simulated using Tanner tool in 0.35µm 2p4m CMOS process technology. The results obtained at $I_{bias} = 100nA$, $I_x = 100nA$, and V_{DD} = $-V_{SS}$= 0.75V. If a sinusoidal signal applied at the input $i_{in}(t) = 60nAsin(2\pi * 10kHz * t)$ and atten=0.5. It is clear from figure (3.4) that the simulated results are in very good agreement with the theoretical one, which confirms the functionality of the developed design.

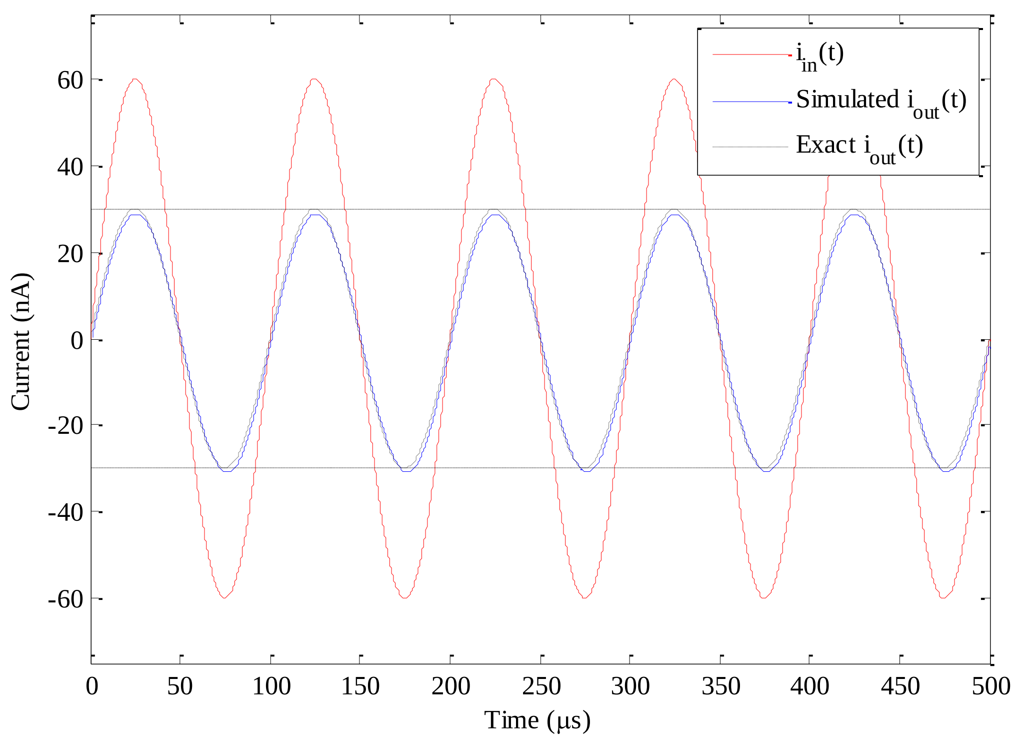


Figure 3.4 Transient response of LCVGA when Atten=0.5

The stability of the design has been tested against temperature variations over 100℃ range (-25℃:75℃). The circuit features 0.0541nA/1 ℃ over this range. Figure (3.5) demonstrates this claim. Up to 10MΩ load has been attached to the output terminal to verify the functionality of the circuit with different loads. As seen in figure (3.6), the circuit shows good performance with reasonable error up to 2.5MΩ. The Total Harmonic Distortion (THD) against different input amplitudes shows that the maximum THD is 3.5% at I_x=100nA and f=10 kHz as shown in figure (3.7).

The response of this structure to the step input presents an appropriate stability behavior whereas the transition time is 4.125μs as illustrated in figure (3.8). Different attenuation values have been taken and the corresponding output signals shown in figure (3.9).

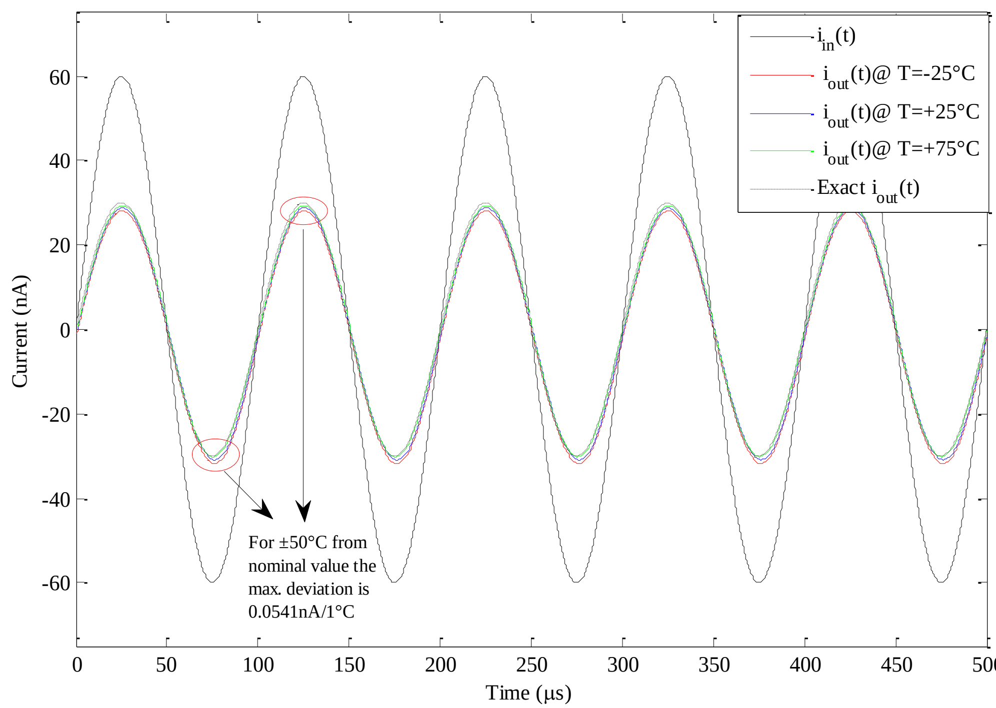


Figure 3.5 Response with different temperatures

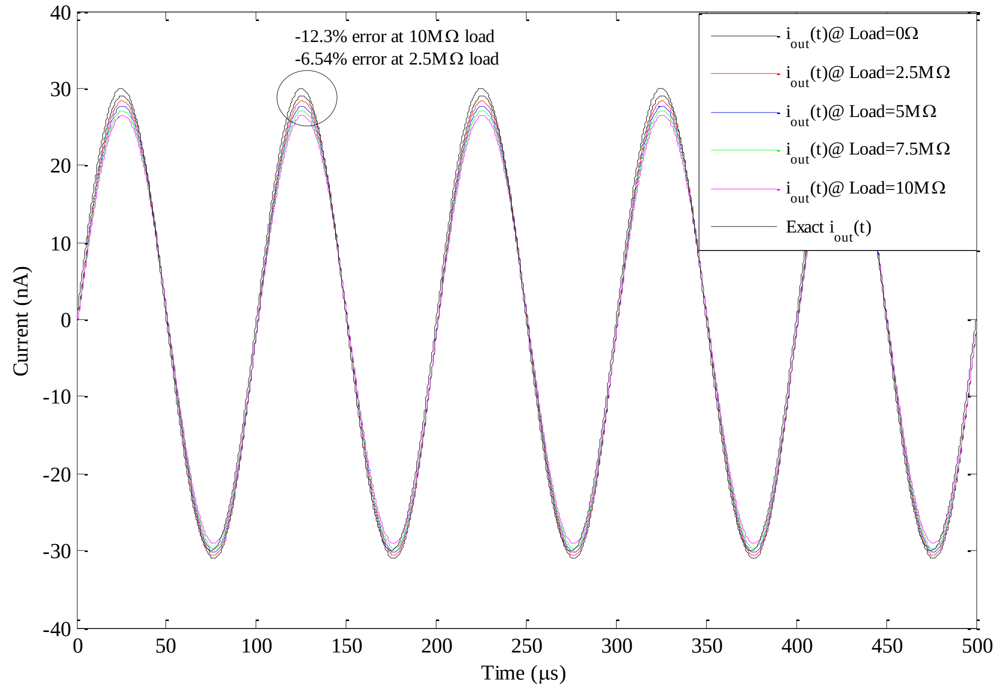


Figure 3.6 Response with different loads

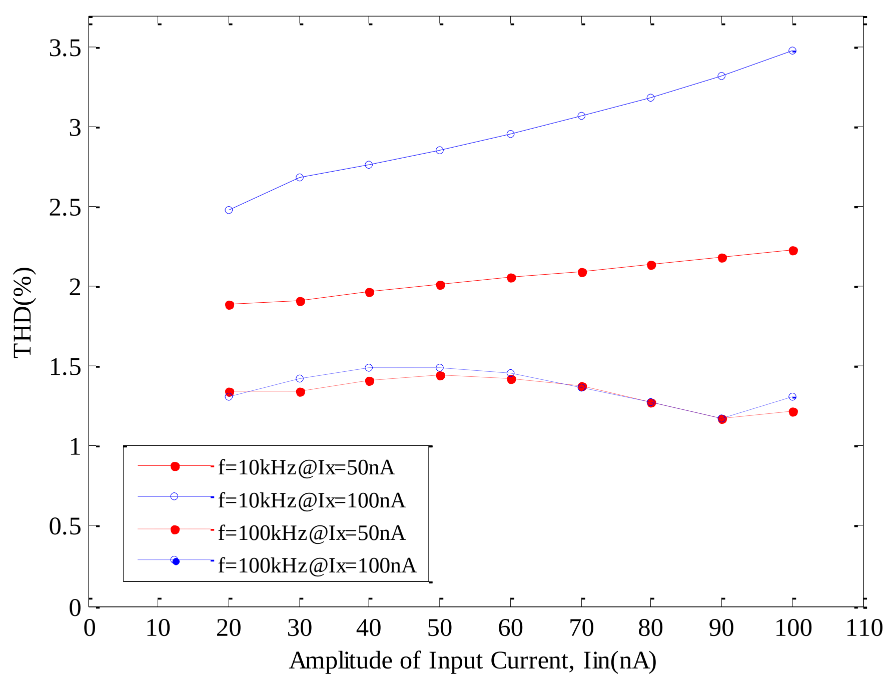


Figure 3.7 THD of LCVGA

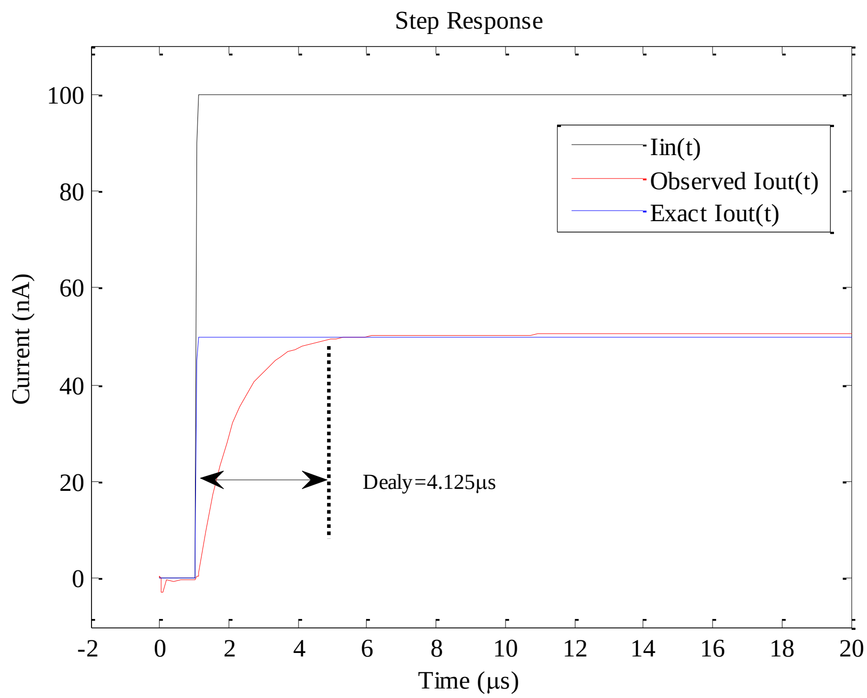


Figure 3.8 Step response of LCVGA

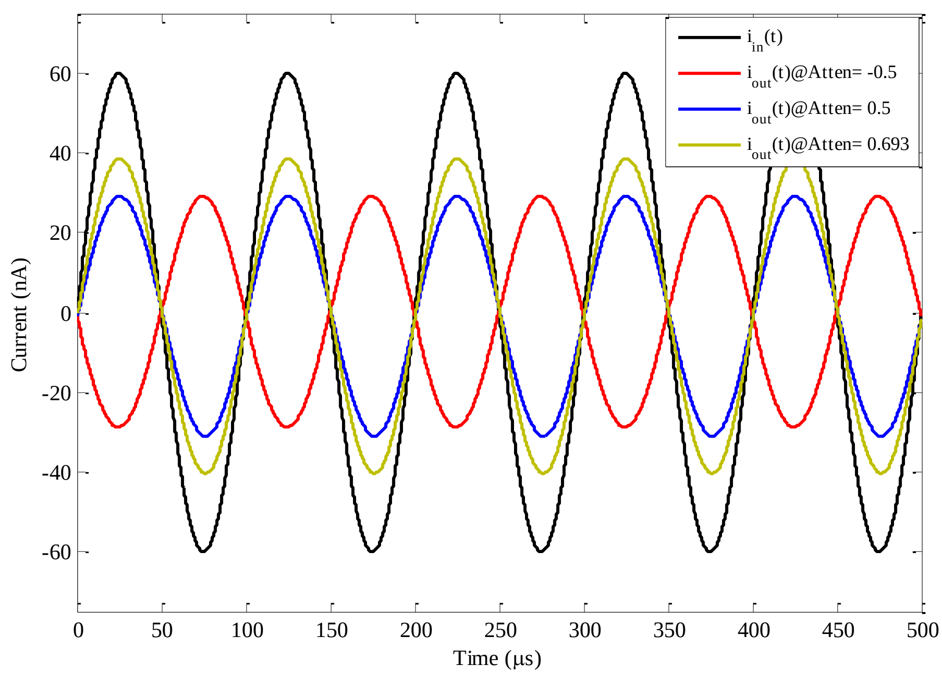
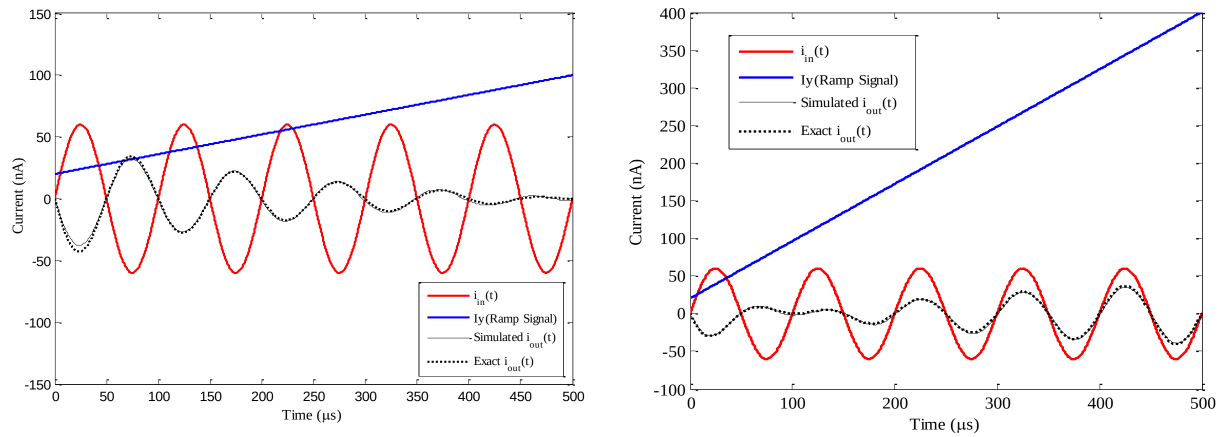


Figure 3.9 i_{out} with different attenuation values

Transient response when i_{in} is a 10 kHz sinusoidal signal and I_{ctrl} is a ramp is shown in figure (3.10); i_{out} is shown to have variable amplitude according to the control signal. Figure (3.11) shows the response when 100 kHz input signal is applied.



(a) (b)

Figure 3.10 Transient response when I_{ctrl} is ramp (a) 80nA p-p (b) 380nA p-p

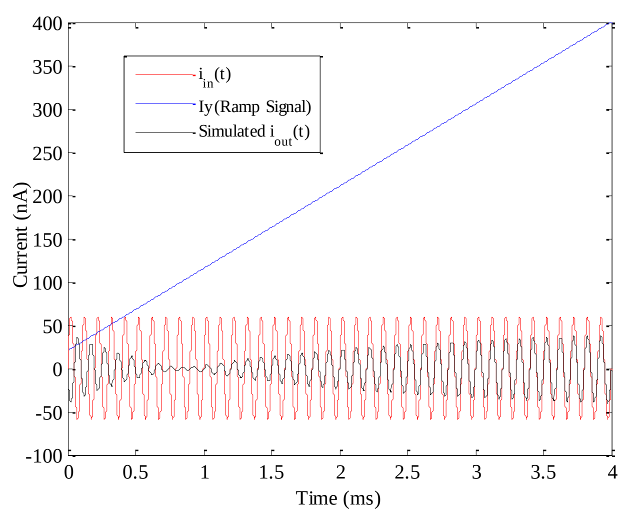


Figure 3.11 Transient response when f_{in}=100 kHz

The response of the circuit when a 380nA peak-to-peak and 80nA peak-to-peak triangular waveform applied is shown in figures (3.12) and (3.13), respectively.

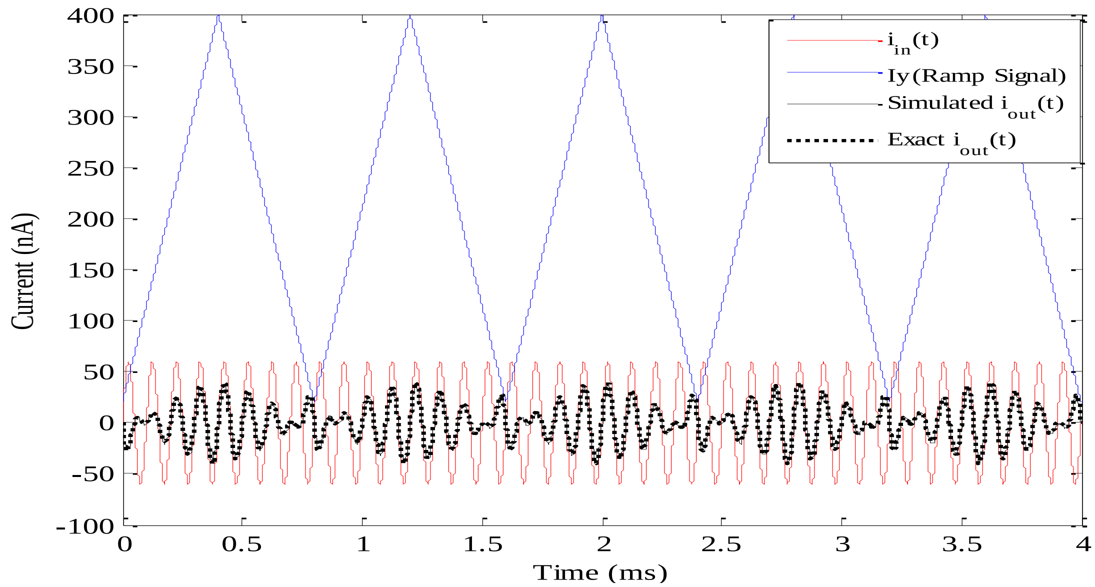


Figure 3.12 380nA peak-to-peak triangular

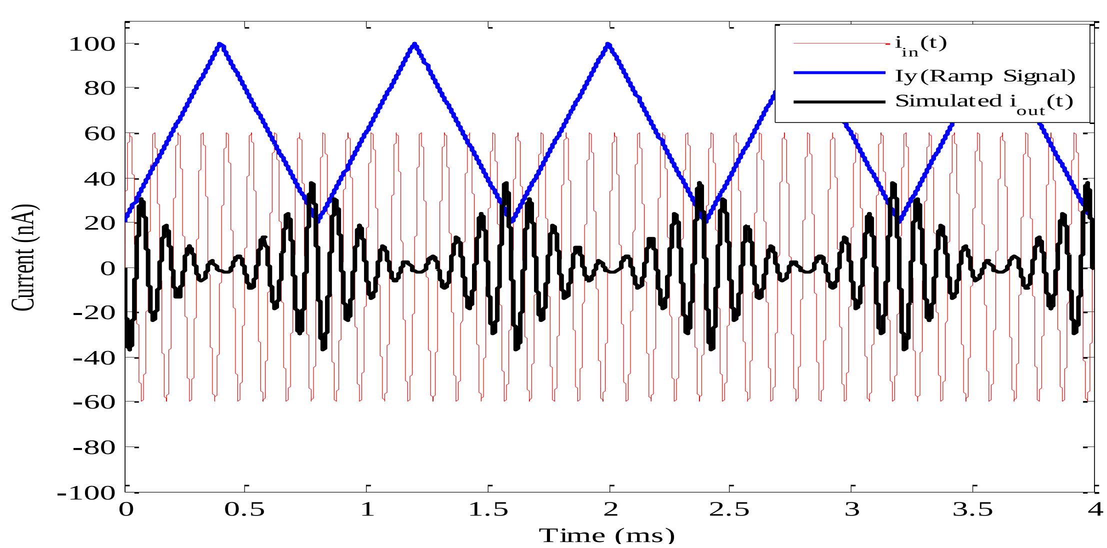


Figure 3.13 80nA peak-to-peak triangular

Simulation for the frequency response of the proposed LCVGA was carried out as shown in figure (3.14). Firstly, 10kΩ resistive load was attached to the output. When atten= -0.5, 0.5 and 0.693 the corresponding cut-off frequency is 30.62MHz, 0.5MHz and 0.36MHz, respectively. Secondly, 50pF capacitive load was attached in parallel with R=10kΩ and for atten= -0.5, 0.5 and 0.693 the corresponding cut-off frequency is 550 kHz, 230 kHz and 205 kHz, respectively. The simulated maximum power consumption for the proposed LCVGA is around 0.857μW. The transistors dimensions are listed in table (3.1) and the summary of the simulation results is listed in table (3.2).

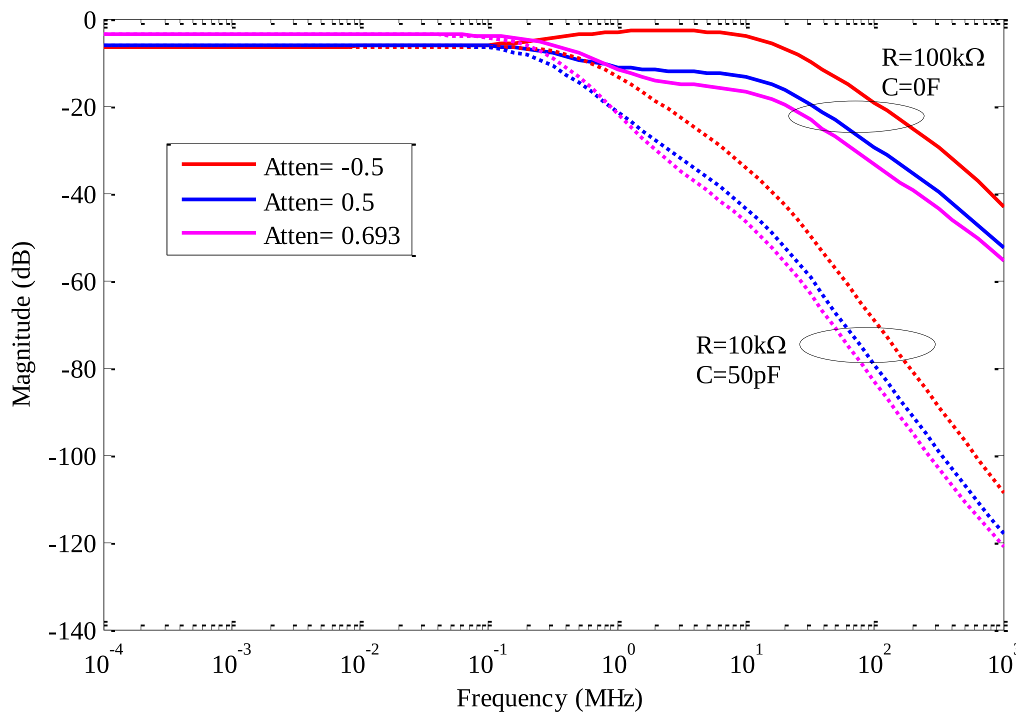


Figure 3.14 The frequency response of the proposed LCVGA

Table 3.1 LCVGA transistors dimensions

Transistor	$\frac{W}{L}$ **(μm/μm)**	**Ratios**
M1, M2, M7, M8	$^{3.5}/_{1.75}$	2
M3, M4, M9, M10	$^{3.5}/_{19.6}$	1/5.6
M5, M6	$^{21}/_{0.35}$	60
M11, M12, M13	$^{14}/_{14}$	1

Table 3.2 Performance summary

Parameter	Proposed LCVGA
Process	0.35μm, 2p4m CMOS
Operation mode	Current-Mode
Voltage Supply	±0.75V
Minimum Atten.	-0.8
Maximum Atten.	0.693
Max. linearity error	5%
BW	30.62MHz @ Atten=-0.5 and 10kΩ resistance load
Power Consumption	0.857μW
THD	3.5%
Applications	e.g. AGCs for Bionic Ears (BE)

3.1.4 Conclusion

In conclusion, a new kind of VGA has been disclosed. It is current-mode OTA-based logarithmic-control VGA (LCVGA). The developed design enjoys simplicity and attractive for integration. This block can be a very useful block in analog signal processing circuits and systems. The design operates from low voltage supply and consumes very small amount of power.

3.2 Exponential-Control VGA

3.2.1 Introduction

The linear-in-dB variable gain amplifier (VGA) is usually employed in Automatic Gain Control (AGC) loop to increase the signal-to-noise ratio (SNR).

Various approaches have been reported to implement VGAs circuits [43, 54-61] and such circuits can be found in several signal processing applications e.g. wireless receivers [54] in order to enhance the system performance regarding the linearity, SNR and power consumption, global positioning system (GPS) receivers [55], disk drives [56], biomedical signal acquisition [57] and direct-conversion receivers [58].

Among the most significant demands of VGAs are the wide range of gain variation, low sensitivity against voltage supply variation, small chip size and consequently low power consumption.

3.2.2 Proposed Exponential-Control VGA

The proposed exponential-control VGA is developed based on the new approximation given in equation (2.45) and its CMOS implementation shown in figure (2.37) chapter 2 with small modification where the control signal was applied to the input of the EXPFG cell and the input small signal has been added to the DC component I_w in the divider included in EXPFG as illustrated clearly in the figure (3.15).

According to Kirchhoff's Current Law (KCL) "the sum of current into a junction equals the sum of current out of the junction", then the current flows through Z node in figure (3.15) will be obtained as shown in equations (3.15)-(3.18):

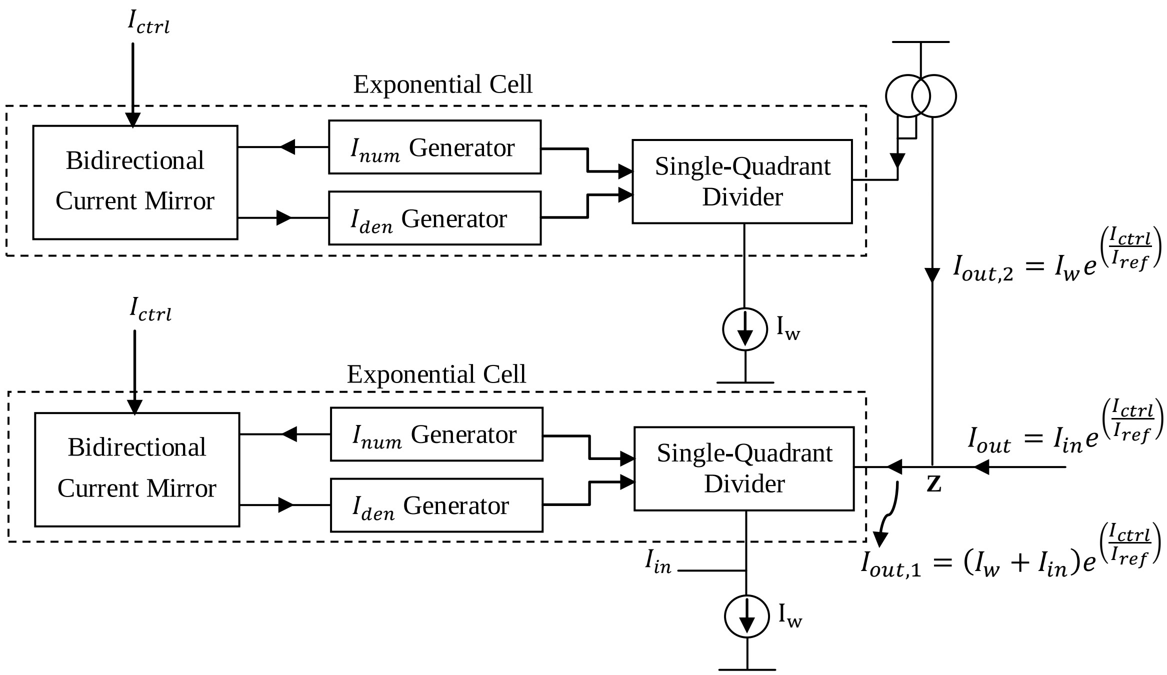


Figure 3.15 The proposed structure of exponential-control VGA

$$I_{out,1} = (I_w + I_{in}) e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)} \tag{3.15}$$

$$I_{out,2} = I_w e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)} \tag{3.16}$$

$$I_{out} = I_{out,1} - I_{out,2} = (I_w + I_{in}) e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)} - I_w e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)} \tag{3.17}$$

$$I_{out} = I_{in} e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)} \tag{3.18}$$

$$A_i = \frac{I_{out}}{I_{in}} = e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)} \tag{3.19}$$

where A_i is the current gain, I_{ctrl} is the control signal and I_{ref} is the reference constant current. From equation (3.18), it is obviously that a variable-gain amplifier can be realized and its gain can be exponentially controlled by the control current I_{ctrl}. This current-mode structure exhibits a linear-in-dB controllable output range of 71 dB with ±0.5 dB linearity error over maximum input control signal -150nA≤ I_{ctrl}≤100nA.

The gain in linear dB scale is calculated as follows:

$$A_i(dB) = 20log_{10}\left(e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)}\right) \tag{3.20}$$

To more simplify equation (3.20), log_{10}- ln relationship can be used as the following:

$$log_{10}(x) = \frac{ln(x)}{ln(10)} \tag{3.21}$$

$$A_i(dB) = 20\frac{ln\left(e^{\left(\frac{I_{ctrl}}{I_{ref}}\right)}\right)}{ln(10)} \tag{3.22}$$

$$A_i(dB) = 8.69\frac{I_{ctrl}}{I_{ref}} \tag{3.23}$$

Equation (3.23) readily shows that the gain in dB scale is linearly proportional to the control signal.

3.2.3 Simulation Results

Simulation results are given to verify the theory of the proposed VGA. Tanner tool is used with standard 0.35μm CMOS process to simulate the proposed structure of exponential-control VGA in figure (3.15). The circuit operates from ±0.75 V voltage supply and the current I_{ref} is set to 25nA. Figure (3.16) shows that the output control range is around 71dB with ±0.5dB linearity error. Different values of I_{ctrl} (-17.33nA, 0nA and 17.33nA) have been used to meet 0.5, 1 and 2 gain values, respectively, and as a result the eventual output signal changed accordingly as shown in figure (3.17).

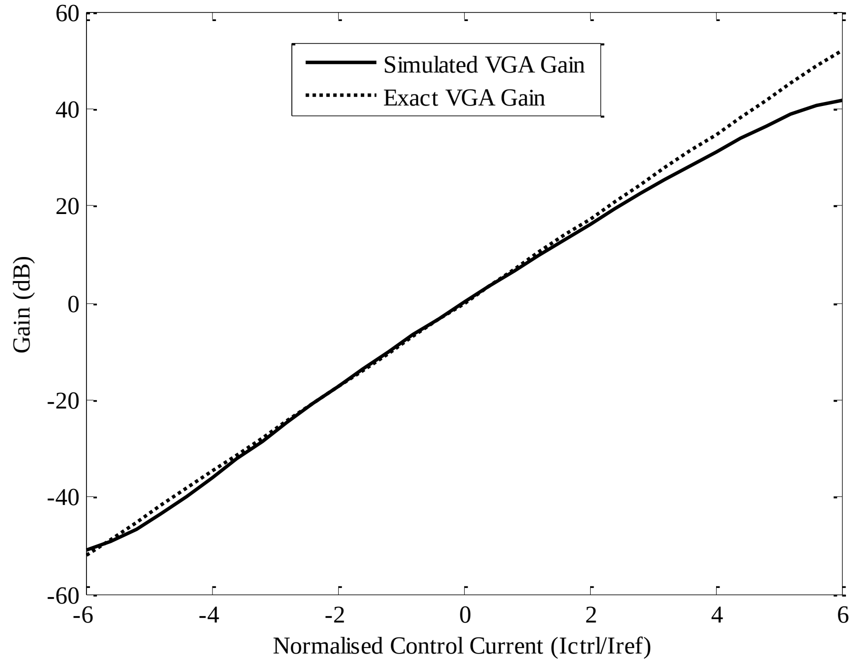


Figure 3.16 Simulation results of the proposed exponential-control VGA

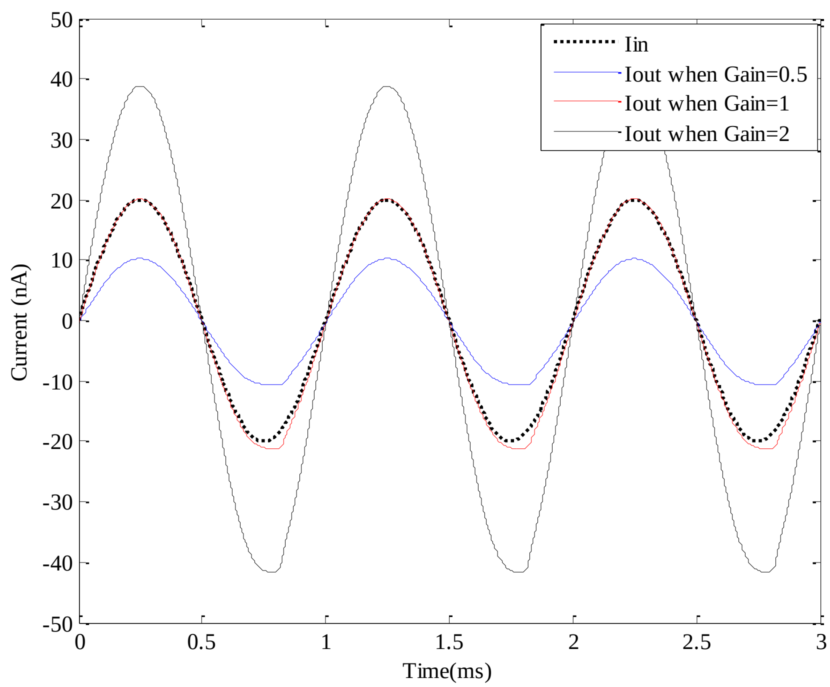


Figure 3.17 Different gain values effect

Transient analysis of the overall circuit is shown in figure (3.18); where I_{in} is a sinusoidal signal with 10 kHz frequency and 20nA amplitude and I_{ctrl} is chosen to be a ramp. The figure demonstrates the variable gain effect on the amplitude of the output current.

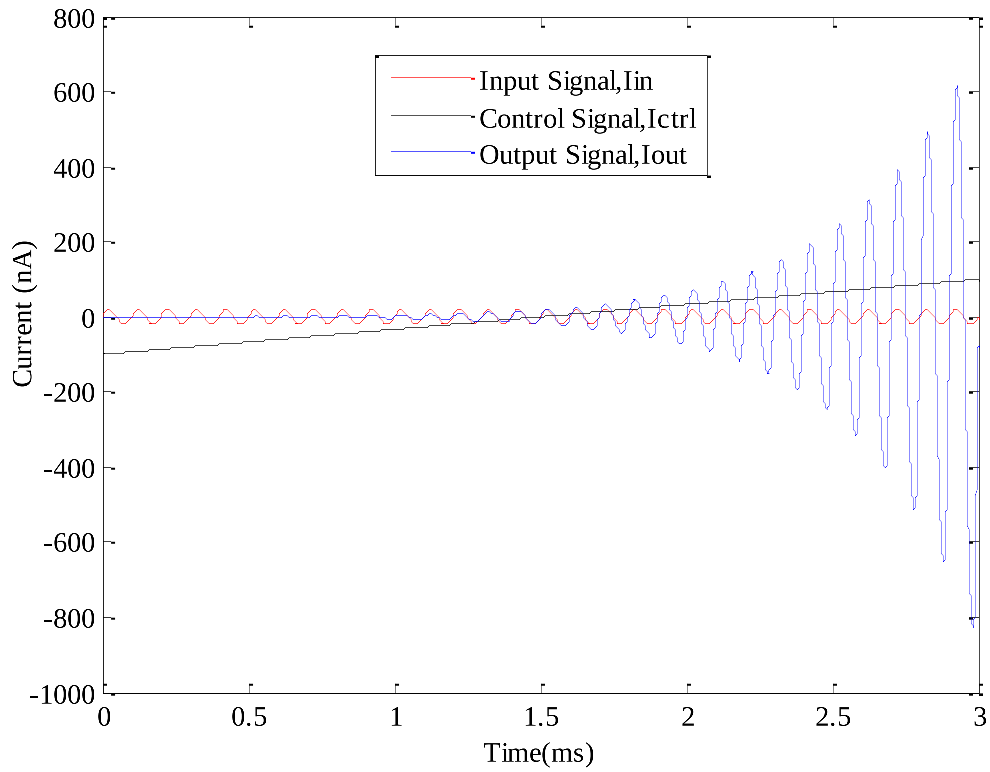


Figure 3.18 Transient analysis of the overall circuit I_{in} is a 10-kHz sinusoidal signal and I_{ctrl} is a ramp. I_{out} is shown to have variable amplitude

The response of the proposed VGA when a sinusoidal input signal with f=10 kHz and 20nA amplitude is applied and the control signal is triangular 200nA peak-to-peak with f=1 kHz and 10 kHz sinusoidal with amplitude of 100nA is shown in figure (3.19) and (3.20), respectively. At point of $I_{ctrl} = 100nA$ the VGA gives highest amplification and $I_{ctrl} = -100nA$ gives highest attenuation.

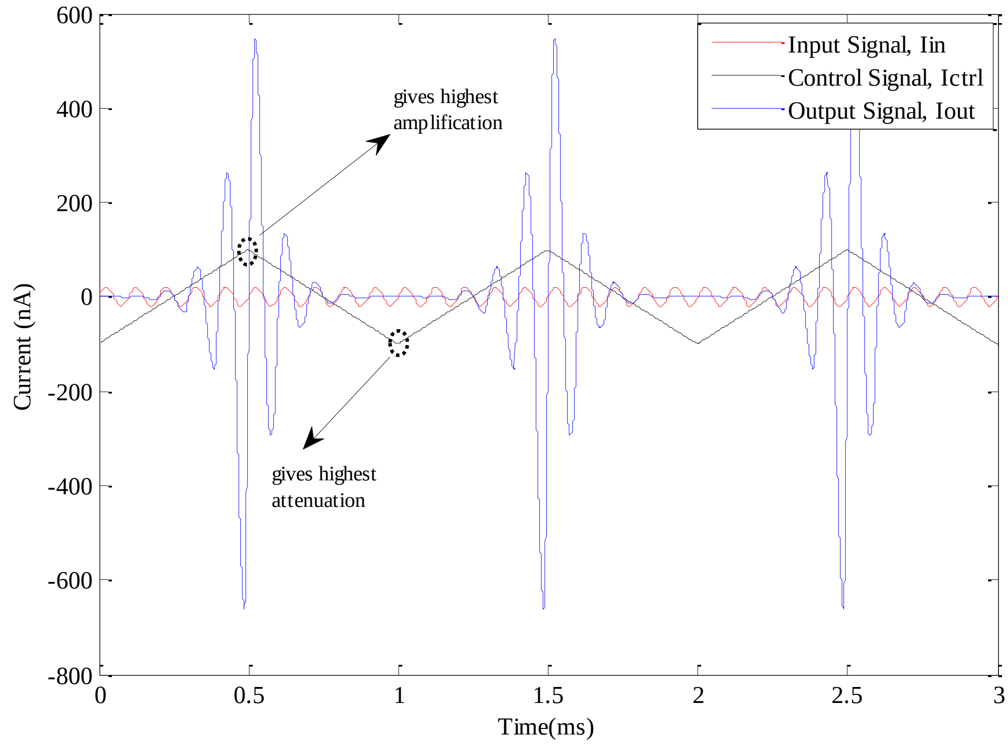


Figure 3.19 VGA response with triangular control signal

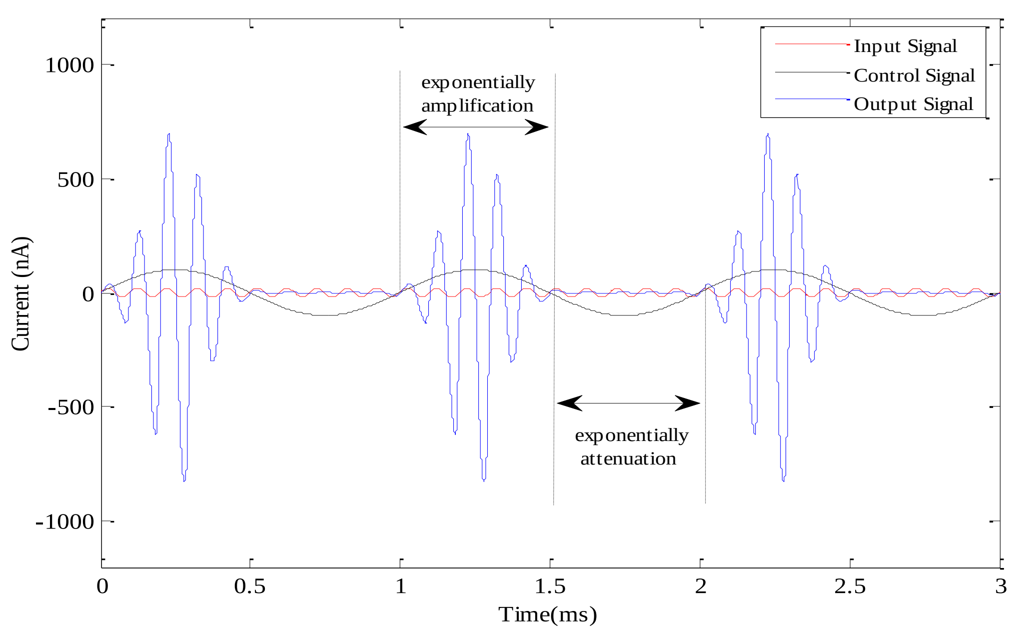


Figure 3.20 VGA response with sinusoidal control signal

The effect of the load and different amplitudes has been studied and simulated by sweeping the load form 0 to 10 MΩ when the amplitude is set to be 40nA and the amplitude of the input varies from 10nA to 50nA when the load set to be 10 kΩ and results are shown in figures (3.21) and (3.22), respectively.

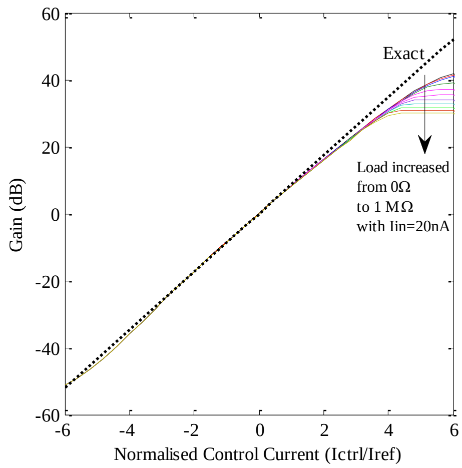


Figure 3.21 Load effect

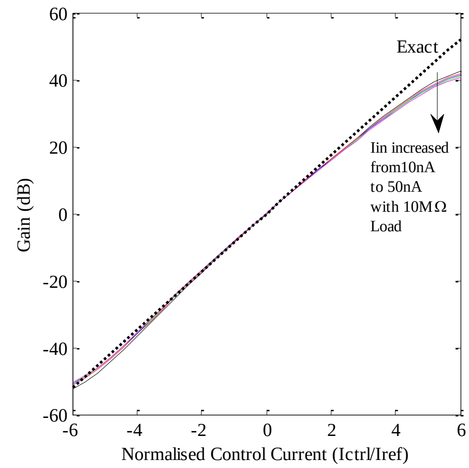


Figure 3.22 Different I_{in} amplitude effect

AC simulation is given in figure (3.23) with resistive (R) and complex (RC) load effect. If R=10kΩ while Gain= 0.5, 1 and 2, the corresponding -3dB frequency is 174 kHz, 242 kHz and 291 kHz, respectively but if C=50pF is added parallel with R, then for Gain= 0.5, 1 and 2 the -3dB frequency is 132 kHz, 170 kHz and 181 kHz, respectively.

Table (3.3) outlines the most features of the proposed VGA compared to the prior works. These performance parameters are either better or compare favorably with the reported state-of-the-art VGAs.

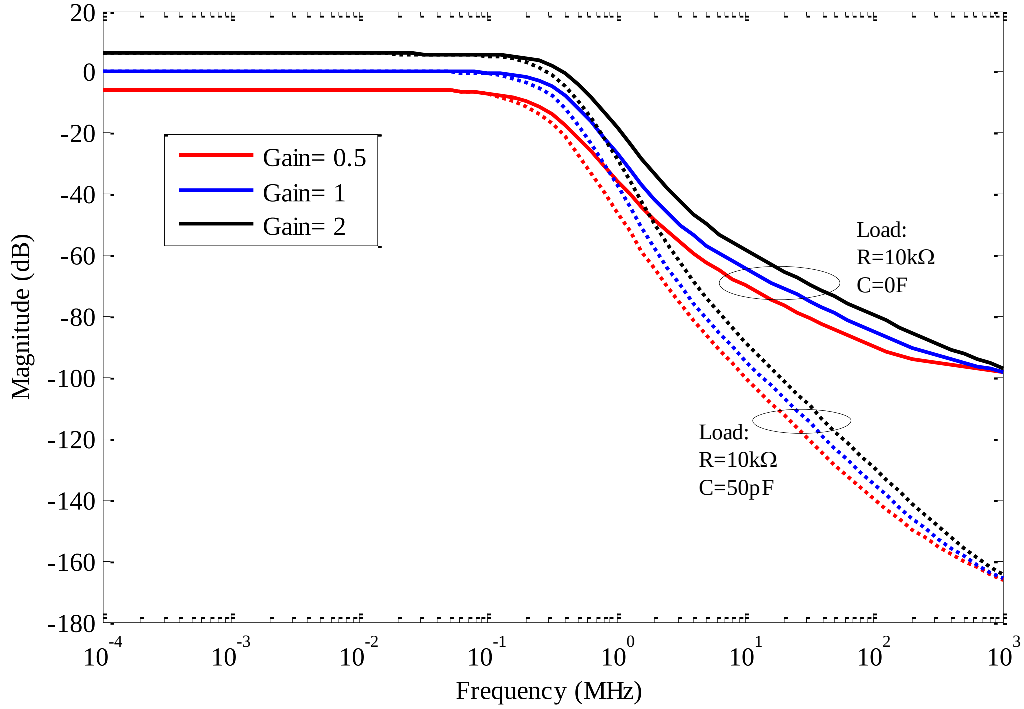


Figure 3.23 AC response

Table 3.3 Comparison with prior works

Parameter	[58]	[59]	[60]	[61]	This Work
Year	2012	2004	2006	2009	2012
Process (CMOS)	0.18µm	0.5µm	0.18µm	0.18µm	0.35µm
Gain (dB)	-3 to 45	-26.79 to 23.94	0 to 95	-10 to 50	-49 to 22
Stages	1	1	3	3	1
Voltage supply	1.8V	2V	1.8V	1.8V	±0.75V
BW	3 MHz	134 kHz	32 MHz	8 MHz	181 kHz [a]
Power consumption	0.549mW	1.6µW	6.48mW	6.7mW	12.782µW

[a] @ RC=0.5µs & Gain=2

CHAPTER 4

LOG-ANTILOG COMPUTATIONAL CIRCUIT

Log-antilog based versatile building block for implementing computational functions such as four-quadrant multiplier, squarer, divider, inverse and cube-law in analog domain is proposed and simulated in 0.35μm 2p4m n-well CMOS process using Tanner tool. The proposed block features current-mode operation and consumes around 13.184μW from ±0.75 V power supply. The linearity error is less than 4.1% and the -3 dB bandwidth of the overall circuit has been observed to over 700 kHz. The total harmonic distortion (THD) is found to be less than 2.25%. Simulation results of all proposed functions are given to verify the theoretical analysis.

4.1 Introduction

Analog computational circuits like multiplier, squarer and divider represent pivotal elements in the design of many integrated circuits for numerous signal processing applications; for example: AM modulators, frequency doublers, equalizers, fuzzy systems, neural networks and etc.

Several computational circuits have been introduced in the previous literature [6, 62-95]. However, many of them are in voltage-mode [62-75], other configurations need at least three times of the threshold voltage, thereby aren't proper for low voltage applications [85-89], consume a relatively large area [83, 90, 91], have limited bandwidth [86-91] and large linearity error [88, 90-95]. The topology proposed in [63] can work for voltage-mode and current-mode but employs floating-gate MOS transistors i.e. require higher supply voltage and it is not suitable for low voltage operation. Since current-mode circuits received more attention than their voltage-mode counterparts, some current-mode configurations are reported in the prior art [6, 76-81]. The most recent work [6] uses MOSFET biased in weak inversion region to introduce computational circuit capable of performing multiplication, division, squaring and 1/x functions. However, the main drawback of this circuit is the limited input range.

In specific applications; cost, small area on the chip, low voltage operation, power consumption, high accuracy and current-mode operation (i.e. wide range of frequencies) are required and necessary for integration as a part of VLSI.

4.2 Proposed Log-Antilog Based Computational Circuit

The developed topology of the computational circuit shown in figure (4.1) is based on the log-antilog cells proposed in chapter (2). According to figure (4.1), two current mirrors, four logarithmic circuits, and two exponential function generators have been used to implement a multifunction current-mode circuit efficient to perform different computational operations in analog domain.

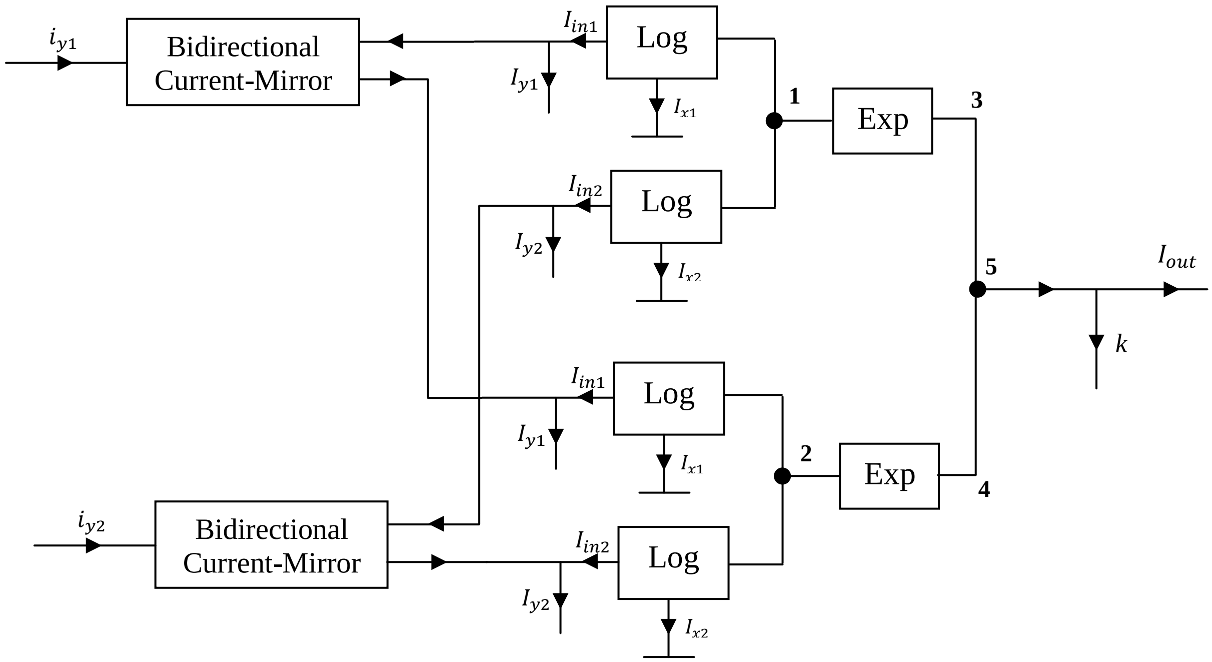


Figure 4.1 Log-Antilog Computational circuit implementation

With the reference to figure (4.1), the current at node 1 and node 3 are shown in equations (4.1) and (4.2) respectively:

$$I_{node1} = \frac{I_{bias}}{2} ln\left(\frac{I_{in1}I_{in2}}{I_{x1}I_{x2}}\right) \tag{4.1}$$

$$I_{node3} = I_w e^{\left(\frac{\frac{I_{bias}}{2} ln\left(\frac{I_{in1}I_{in2}}{I_{x1}I_{x2}}\right)}{I_{ref}}\right)} \tag{4.2}$$

Using the properties of logarithmic exponential functions will result in:

$$\boxed{I_{node3} = I_w \left(\frac{I_{in1}I_{in2}}{I_{x1}I_{x2}}\right)^{\propto}} \tag{4.3}$$

Where $\alpha = \frac{I_{bias}}{2I_{ref}}$ is the power factor ratio, I_{in1}, I_{in2}, I_{x1} and I_{x2} are the input signals, and I_w is constant current used to scale the output signal. Clearly, equation (4.3) is efficient to implement different computational functions like multiplication, division, squaring, inverse, raise to power and parametric current amplifier. In order to demonstrate the feasibility of the proposed circuit in figure (4.1) and equation (4.3), simulation results for different functions has been carried out using Tanner tool in 0.35µm n-well 2p4m CMOS process.

4.3 Four-Quadrant Multiplier

To implement four-quadrant multiplier, design ∝=1 by choosing $I_{bias} = 2I_{ref}$ in equation (4.3). According to figure (4.1), the current flows in the different nodes will be as follows:

$$I_{in1}^{+} = (I_{y1} + i_{y1}) \tag{4.4}$$

$$I_{in2}^{+} = (I_{y2} + i_{y2}) \tag{4.5}$$

$$I_{in1}^{-} = (I_{y1} - i_{y1}) \tag{4.6}$$

$$I_{in2}^{-} = (I_{y2} - i_{y2}) \tag{4.7}$$

$$I_{node1} = \frac{I_{bias}}{2} ln\left(\frac{(I_{y1}+i_{y1})(I_{y2}+i_{y2})}{I_{x1}I_{x2}}\right) \tag{4.8}$$

$$I_{node2} = \frac{I_{bias}}{2} ln\left(\frac{(I_{y1}-i_{y1})(I_{y2}-i_{y2})}{I_{x1}I_{x2}}\right) \tag{4.9}$$

$$I_{node3} = I_w \left[\frac{I_{y1}I_{y2}+I_{y1}i_{y2}+I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right] \tag{4.10}$$

$$I_{node4} = I_w \left[\frac{I_{y1}I_{y2}-I_{y1}i_{y2}-I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right] \tag{4.11}$$

$$I_{node5} = \frac{2I_w i_{y1}i_{y2}}{I_{x1}I_{x2}} + k \tag{4.12}$$

where $k = \frac{2I_w I_{y1} I_{y2}}{I_{x1} I_{x2}}$, is the DC component which shifts the ac small signal. Subtracting k in equation (4.12) to get:

$$I_{out} = \frac{2I_w i_{y1} i_{y2}}{I_{x1} I_{x2}} \tag{4.13}$$

From equation (4.13) and if i_{y1} and i_{y2} are the input current signals, a current-mode four-quadrant analog multiplier can be obtained and its output current, I_{out} can be scaled by any of the constant currents I_w, I_{x1} or I_{x2}.

The simulation was carried out with the voltage supply ±0.75 V and the aspect ratios of all transistors of sub-circuits as indicated in chapter 2. With $I_{y1} = I_{y2} = 150nA$, $I_{x1} = I_{x2} = 130nA$ and $I_w = 10nA$, when the input current i_{y1} varies from -100nA to 100nA while the input current i_{y2} steps from -100nA to 100nA by 20nA, the results of DC transfer characteristic of the proposed analog 4-Q multiplier is shown in figure (4.2). The maximum linearity error is around 1.8%.

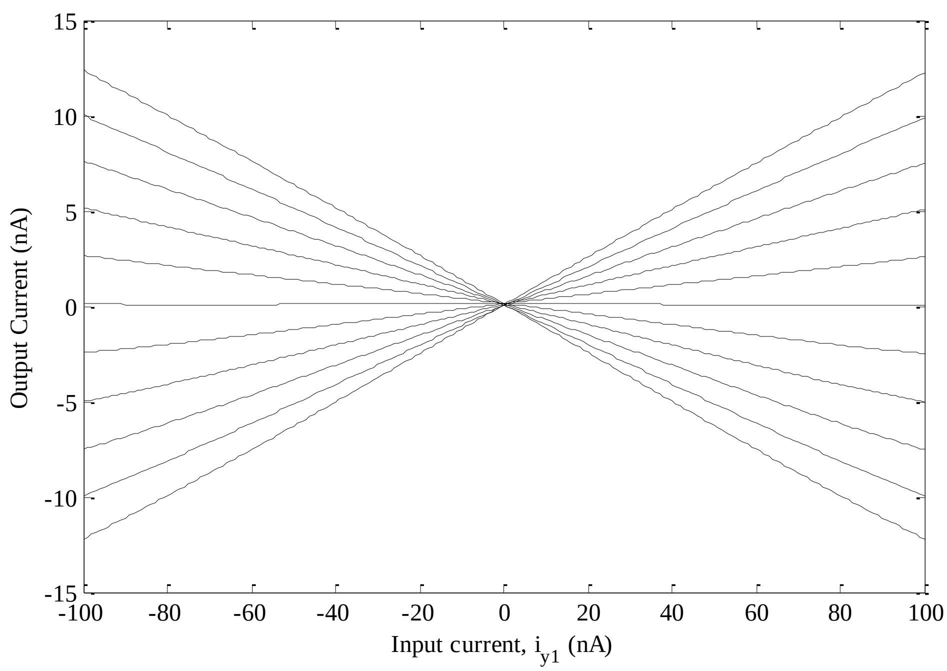


Figure 4.2 DC transfer characteristics of the proposed 4-Q multiplier

The proposed multiplier can be utilized as an amplitude modulator (AM). If the input waveforms are $i_{y1} = A\sin(2\pi f_1 t)$ and $i_{y2} = A\sin(2\pi f_2 t)$, where A=100nA is the amplitude of the waveforms, i_{y1} is the carrier waveform with f_1=10 kHz and i_{y2} is the modulating waveform with f_2=1 kHz, respectively, the output modulated waveform I_{AM} is clearly shown in figure (4.3). It has the same frequency of i_{y1} but its amplitude changed according to i_{y2} . Figure (4.4) illustrates the functionality of the proposed multiplier as AM modulator when the modulating waveform i_{y2} is a rectangular signal with 200nA peak-to-peak and 1 kHz frequency.

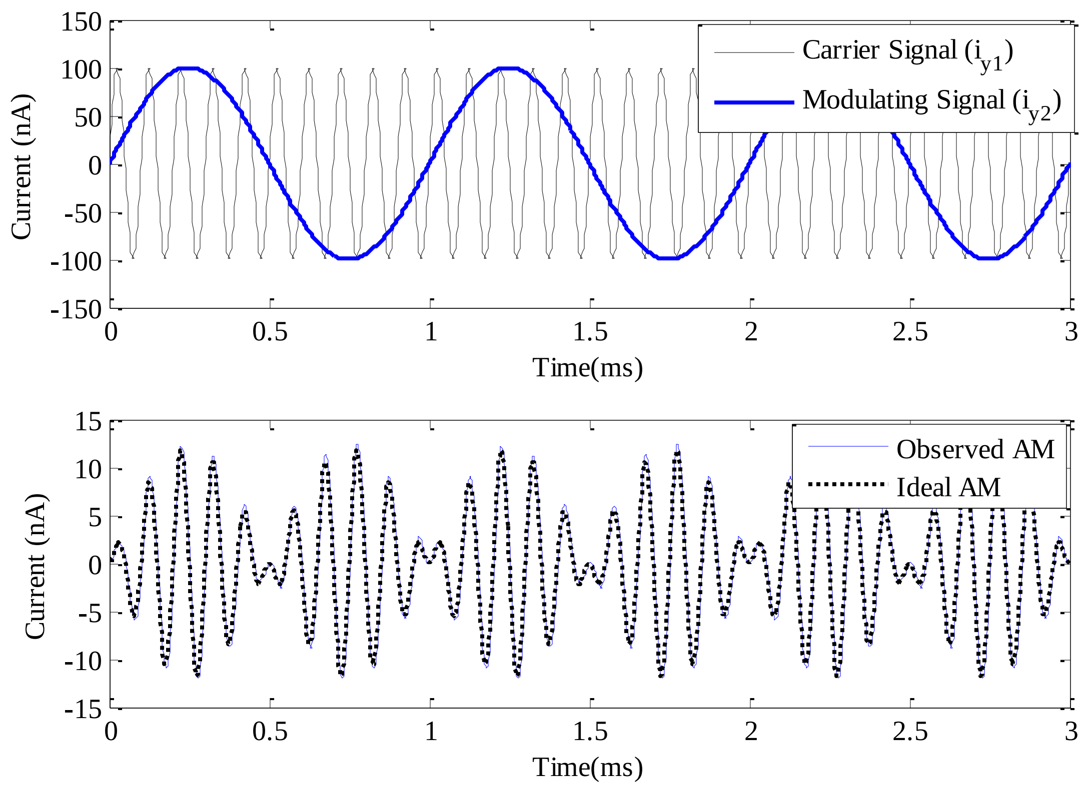


Figure 4.3 The proposed multiplier is used as a modulator

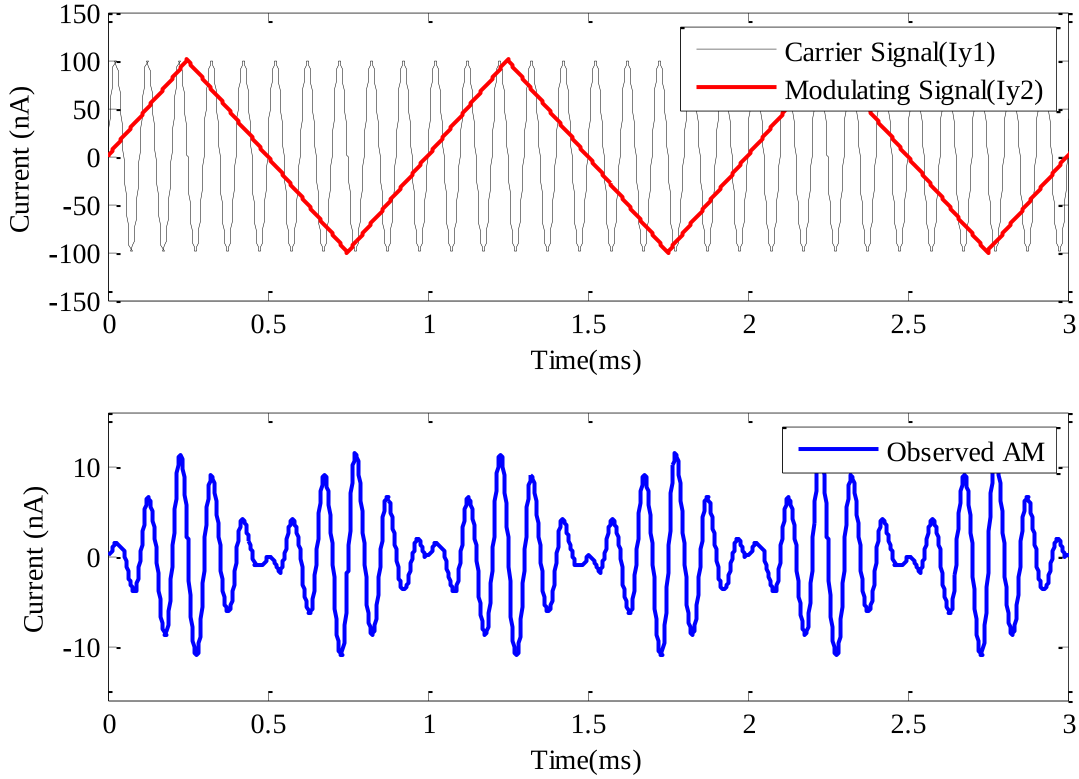


Figure 4.4 AM modulator with rectangular i_{y2}

The frequency response of the proposed multiplier is shown in figure (4.5). If 10kΩ resistance load was attached to the output terminal and the capacitance load was set to 0, 20pF, 40pF, 60pF, 80pF and 100pF, the corresponding -3-dB bandwidth is about 722 kHz, 681 kHz, 609 kHz, 587 kHz, 536 kHz, and 516 kHz, respectively. The main cause for the restricted bandwidth of the proposed design is due to the subthreshold limitations.

The total harmonic distortion (THD) of the circuit in figure (4.1) is shown in figure (4.6). The maximum THD is 2.25%. The simulated power consumption is around 10μW

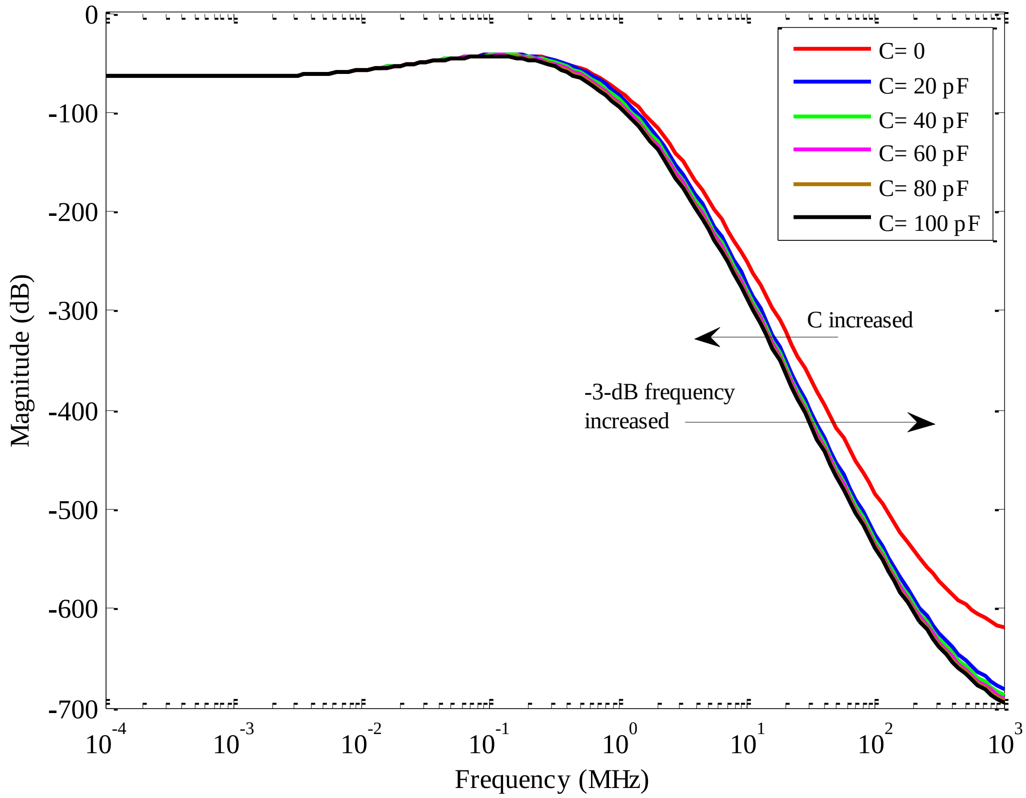


Figure 4.5 Frequency response of the proposed circuit in figure (4.1)

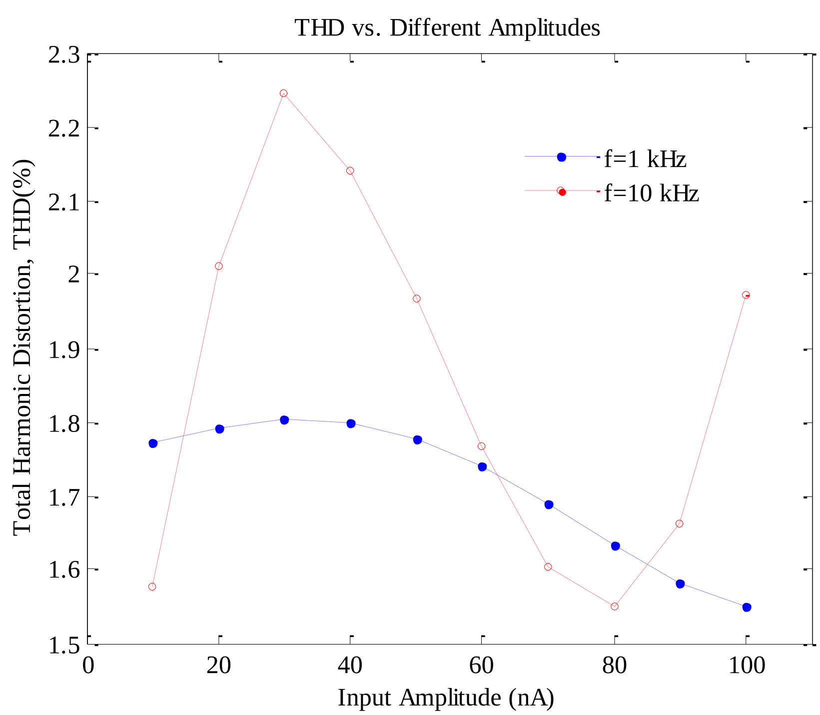


Figure 4.6 THD of the output waveform for different input amplitudes

4.3.1 Mismatch effect

Referring to equations (4.3) and (4.12), if I_{bias} is not exact equal to $2I_{ref}$ {i.e. ($I_{bias} = 2I_{ref} + \Delta I$) $\rightarrow$ ($\propto = 1 + \Delta\propto$)} and if k is not exact (i.e. $k = \frac{2I_w I_{y1} I_{y2}}{I_{x1} I_{x2}} + \Delta k$), then the output current expressed in equation (4.13) can be rewritten as indicated in equation (4.14):

$$I_{out} = \frac{2I_w i_{y1} i_{y2}}{I_{x1} I_{x2}} + \Delta k + \Delta\delta \frac{I_w\left(I_{y1} I_{y2} + i_{y1} i_{y2}\right)}{I_{x1} I_{x2}} + (\delta_1 - \delta_2) \frac{I_w\left(I_{y1} i_{y2} + I_{y2} i_{y1}\right)}{I_{x1} I_{x2}} \tag{4.14}$$

where:

$$\delta_1 = \left[\frac{I_{y1} I_{y2} + I_{y1} i_{y2} + I_{y2} i_{y1} + i_{y1} i_{y2}}{I_{x1} I_{x2}}\right]^{\Delta\propto}$$

$$\delta_2 = \left[\frac{I_{y1} I_{y2} - I_{y1} i_{y2} - I_{y2} i_{y1} + i_{y1} i_{y2}}{I_{x1} I_{x2}}\right]^{\Delta\propto}$$

$$\Delta\delta = (\delta_1 + \delta_2) - 2$$

$$\Delta\propto = \frac{\Delta I}{2I_{ref}}$$

Inspection of equation (4.14) clearly shows that the output current of the computational circuit comprises four current components. The desired component that is proportional to the multiplication of the input signals in addition to three undesired components. The first undesired component is a constant current component and the other two undesired components are a current proportional to the input current. (See appendix A for the full derivation).

4.4 Squarer

The squaring function can be obtained easily from equation (4.13) by imposing the input currents to be $i_{y1} = i_{y2} = i_y$, and then equation (4.13) can be rewritten as (4.15)

$$I_{out} = \delta i_y^2 \tag{4.15}$$

where $\delta = \frac{2I_w}{I_{x1}I_{x2}}$ is a constant quantity used to scale the output signal. It is evident from equation (4.15) that the squaring function is implementable. To demonstrate the validity of equation (4.15), simulation results using Tanner tool are given with 0.35µm CMOS process technology. The squaring DC transfer curve is shown in figure (4.7). The output signal is in very good agreement with the expected signal with 0.1 nA offset due to the mismatched devices.

The proposed squaring circuit can be employed as a frequency doubler. By using the following Power-Reducing Identification

$$sin^2(\alpha) = \frac{1}{2}[1 - \cos(2 \propto)]$$

and if the input signal, i_y, has the frequency $f_{in} = 1kHz$, the output signal with $f_{out} = 2kHz$ can be obviously seen in figure (4.8). Figure (4.9) shows the output squaring signal if a 200nA peak-to-peak triangular signal with f=1 kHz has been applied at the input.

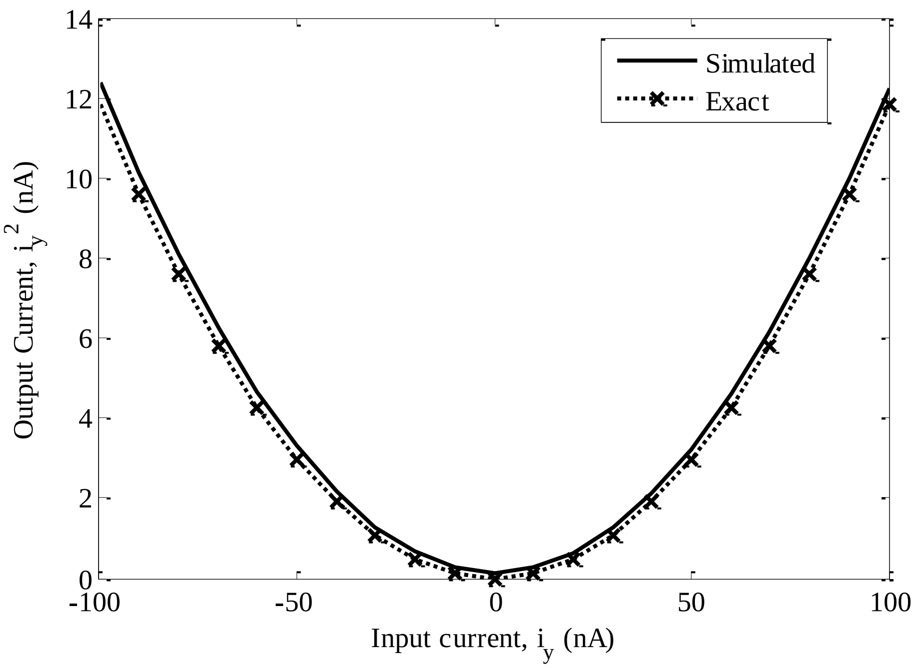


Figure 4.7 Squaring DC transfer characteristics

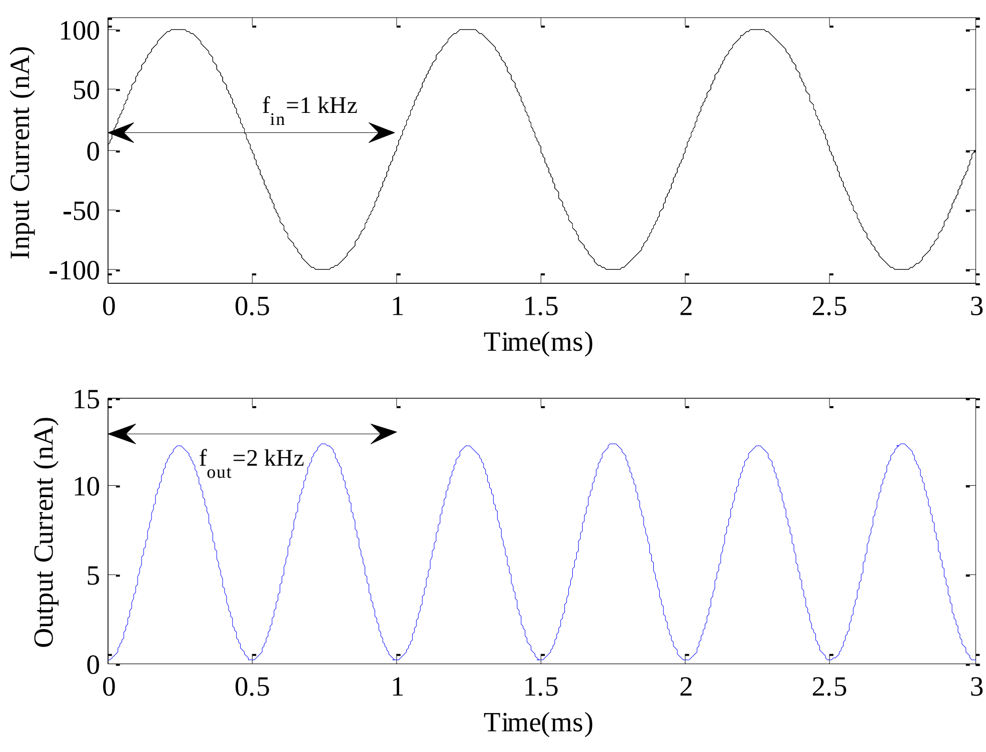


Figure 4.8 The proposed circuit is used as a frequency doubler

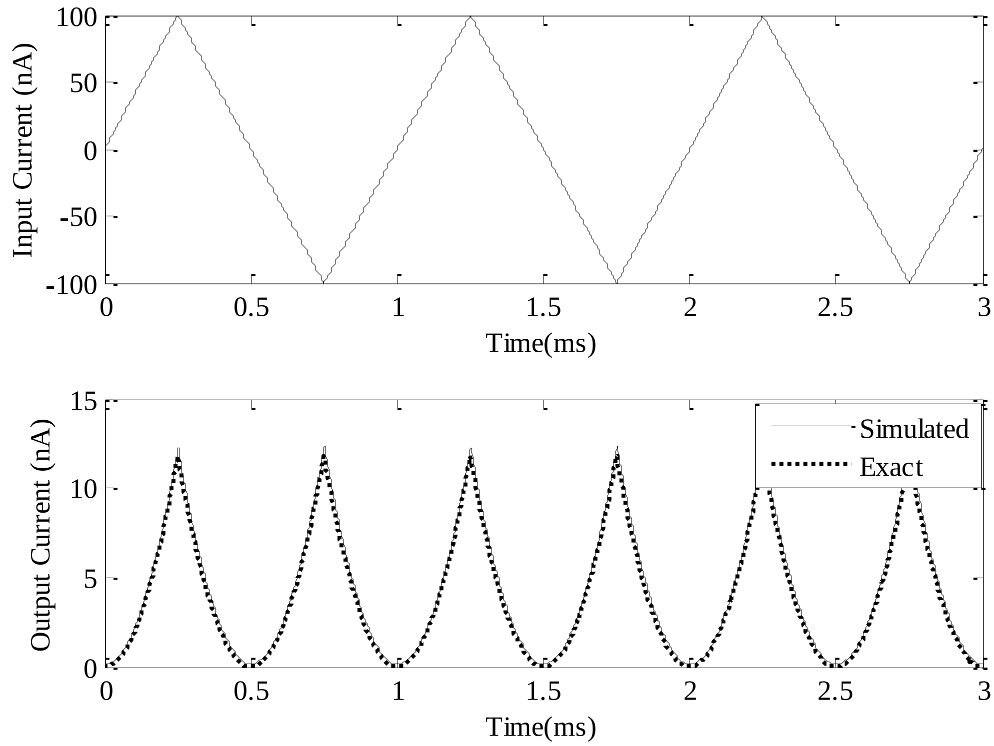


Figure 4.9 Squaring response with a triangular input signal

4.5 Divider

With reference to the equation (4.13), if i_{y2} (numerator) is the dividend and I_{x2} (denominator) is the divisor, and keeping all other currents fixed, then the output current (quotient) is given by:

$$I_{out} = \sigma \frac{i_{y2}}{I_{x2}} \tag{4.16}$$

where $\sigma = \frac{2I_w i_{y1}}{I_{x1}}$ kept constant. From equation (4.16), a two-quadrant divider (2-Q) can be realized in current-mode operation. The simulation of the DC characteristics is shown in figure (4.10), where the dividend, i_{y2} varies from -100nA to 100nA and the divisor, I_{x2} steps from 100nA to 200nA by 10nA. According to the results, the maximum linearity error is 4.1%.

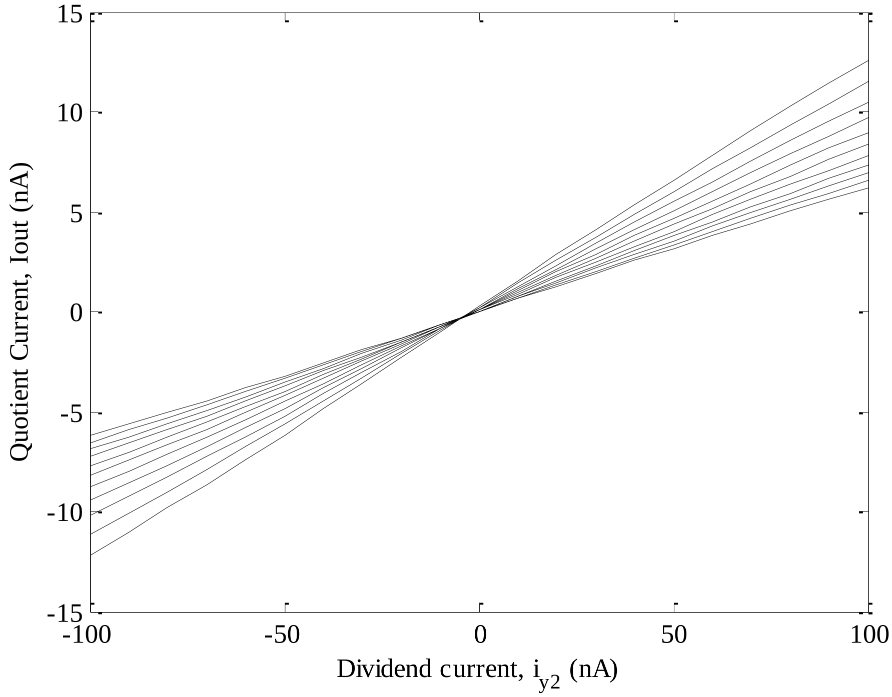


Figure 4.10 DC input/output transfer curves of the 2-quadrant divider

The transient response results are shown in figure (4.11), (a) and (b) for triangular and sinusoidal signals, respectively.

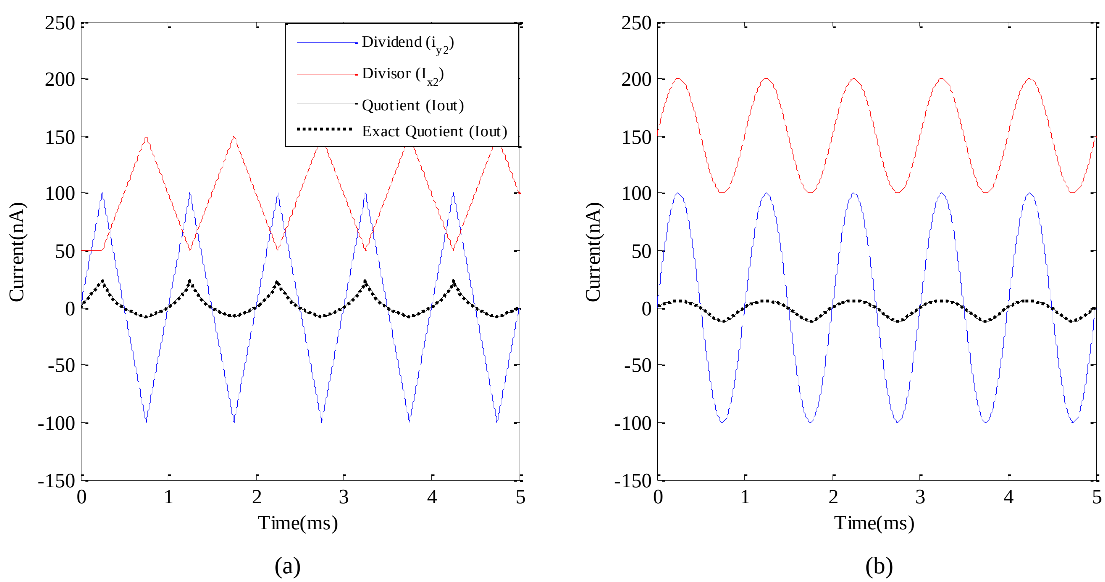


Figure 4.11 Transient response (a) triangular (b) sinusoidal

4.6 1/x Function

The inverse operation is a special case from the division one. So, with keeping i_{y2} constant in equation (4.15), the output current is, therefore, proportional to the inverse of the current I_{x2} and as a result the equation (4.16) will be in the equation (4.17) form:

$$I_{out} = \lambda \frac{1}{I_{x2}} \tag{4.17}$$

where $\lambda = \frac{2I_w i_{y1} i_{y2}}{I_{x1}}$ is the constant term. The simulation results are illustrated in figure (4.12) where I_{x2} varies from 10nA to 300nA while i_{y2} varied from -200nA to 200nA in steps of 25nA.

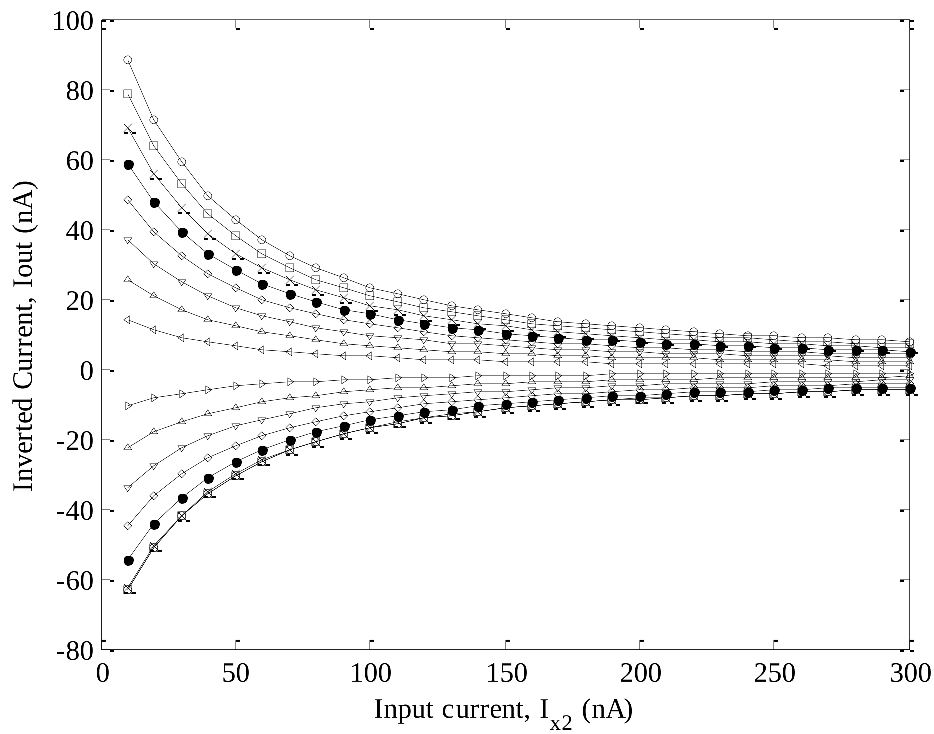


Figure 4.12 Simulation results of 1/x function with different i_{y2}

4.7 Cube-Law Function

According to figure (4.1) and equation (4.3), if $\propto$ is chosen to be equal to $\frac{3}{2}$. Setting $I_{bias} = 3I_{ref}$, $I_{x1} = I_{x2}$ and $I_{in1} = I_{in2} = I_{in}$, then the equation (4.3) can be rewritten as follows:

$$I_{node,3} = \frac{I_w}{I_x^3} \cdot (I_{in})^3 \tag{4.18}$$

From equation (4.18), the current at node 3 in figure (4.1) is proportional to the cubic of the input current. A pure cube-law circuit can be readily realized from the equation (4.18) by using a couple of them in a balanced structure and additional circuit will be added for constant shift compensation. The proposed cube-law design has low power-consumption (13.3μW) and it is also operates under low voltage supply (±0.75 V) but the drawback of this circuit is that the error is relatively significant (12%). The simulation of the cube-law design is displayed in figure (4.13) where a triangular input signal with 200nA p-p has been applied.

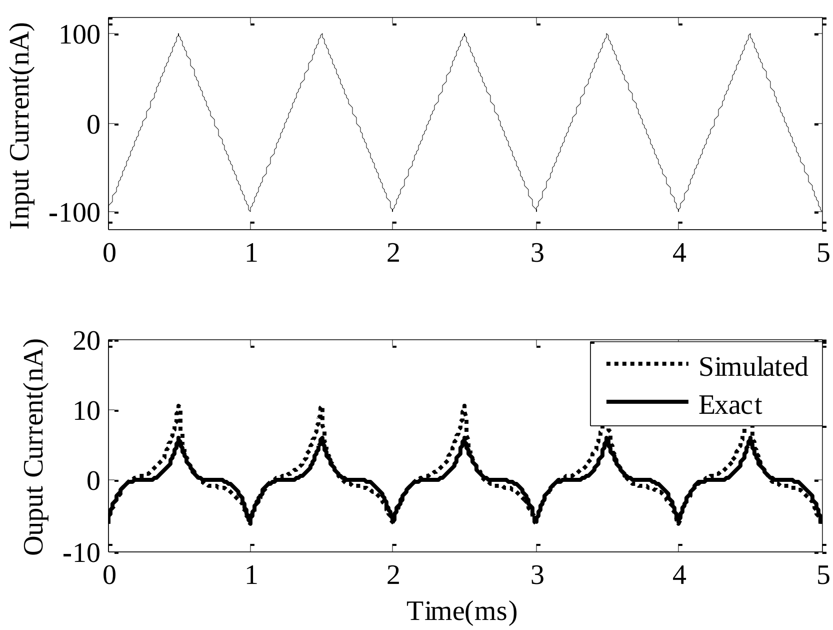


Figure 4.13 Triangular response of the proposed cube-law circuit

4.8 Multi-input Analog Multiplier (MIM)

In the field of analog signal processing, sometimes, it is needed to multiply multiple signals simultaneously [96]-[98]. The conventional way to achieve this necessity is shown in figure (4.14). Depending of the number of inputs, the multiplier circuits are cascaded. Unfortunately, this method increases error at the output, because multiplication naturally is an additive operation. Therefore the noise which is generated in the first stage of the multiplier will be amplified in the next stages [99].

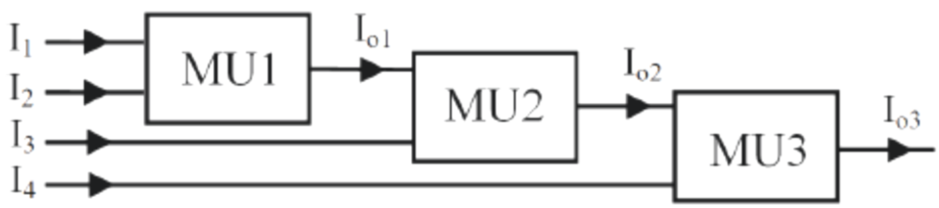


Figure 4.14 Conventional multi-input multiplier

With Log-Antilog properties a multiple input multiplier can be easily obtained. To demonstrate this claim, a novel multiple input analog multiplier has been developed as indicated in figure (4.15) where four input currents can be multiplied simultaneously. Only four simple parallel logarithmic circuits in series with one exponential generator (proposed in chapter 2) have been used. Simulation results have been carried out and figure (4.16) confirms the functionality of the proposed design.

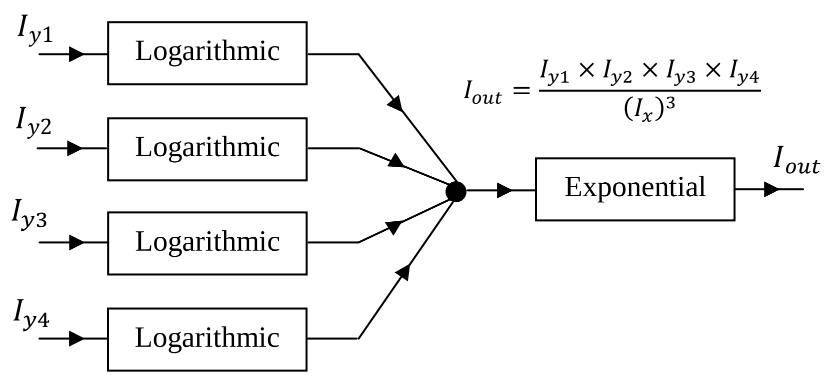


Figure 4.15 The proposed block diagram which can multiply 4 input currents

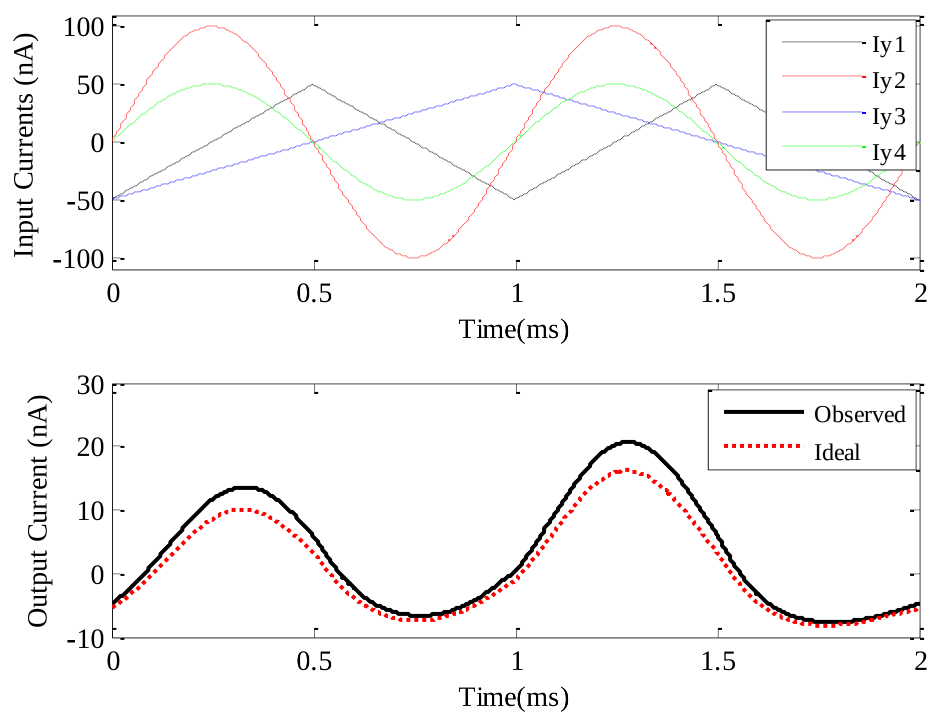


Figure 4.16 Simulation results of MIM structure

The performance of the proposed log-antilog computational circuit compared to recently published works is shown in table (4.1).

Table (4.1) Performance comparison

Parameter	[6]	[62]	[95]	This Work
Year	2012	2010	2005	2012
Functions	Multiplication, squaring, division and inverse	Multiplication	Multiplication	Multiplication, squaring, division, inverse, cube-law MIM multiplier
Technique	Translinear loops	new design principle	Translinear loops	Log-antilog
Operation Mode	Current-mode	Voltage-mode	Current-mode	Current-mode
CMOS Process	0.35μm	0.35μm	0.35μm	0.35μm
Supply Voltage	±0.75V	2V	2V	±0.75V
Linearity error	0.3%	3.2%	5%	1.8% (multiplier)
-3 dB BW	2.3MHz	268 kHz	200 kHz	722 kHz
THD	0.7%	4.2%	0.9%	2.25%
Power Consumption	2.3μW	6.7μW	5.5μW	13.184μW

CHAPTER 5

CONCLUSION AND FUTURE WORK

The use of MOSFETs operating in weak inversion region in designing analog computational circuits has been investigated. In this regard, two new current-mode logarithmic function circuits have been proposed in addition to current-mode exponential function generator. To confirm the validation of the proposed non-linear blocks, different structures for various applications were presented. Firstly, two kinds of variable-gain amplifiers have been developed. Secondly, log-antilog computational circuit efficient to perform multiple arithmetical operations in analog domain has been introduced.

5.1 Conclusions

MOSFETs operating in weak inversion region have proved to be feasible and effective in designing different circuits for analog signal processing applications and as such the main attractive parameters are the low voltage operation, small area on the chip and ultra low power consumption. From this fact, MOSFETs operating in this region is receiving more attention especially in biomedical applications where the power consumption is a key parameter.

In this thesis, the MOSFETs operating in weak inversion region have been utilized to design two current-input current-output logarithmic function circuits. The proposed circuits feature with simplicity, suitable for low voltage environment, stable with temperature and process variations.

Moreover, new exponential approximation has been presented to achieve large output range around 96dB while keeping the error amount less than ±0.5dB. This approximation has been implemented by MOSFETs using translinear loops.

To investigate the capability of the logarithmic and exponential circuits, different log-antilog applications have been presented and simulated.

Two kinds of variable-gain amplifier; logarithmically-control variable-gain attenuator (LCVGA) and exponential-control variable-gain amplifier are introduced.

Finally, computational circuit based on logarithmic exponential cells has been presented in order to perform numerous arithmetical operations.

5.2 Directions for Future Work

Since nothing is perfect and complete in this life, this work can be improved and expanded in some directions.

- Introducing the physical layout of the exponential function generator and then the layout of the overall computational circuit and VGAs.
- Fabrication of these circuits and testing them experimentally to demonstrate the validity of the theory and simulation.
- Implement the exponential current-mode circuit with MOSFET in strong inversion and then build a VGA with very high gain by cascading more than one stage.

Appendix A

Chapter 2:

Referring to the figure (2.27), if the current mirror $1.6I_{ref}$ is not exact (i.e. $1.6I_{ref} + \Delta I_{ref}$), then equations (2.53) and (2.54) can be rewritten as:

$$I_{num} = \left(1.6I_{ref} + \Delta I_{ref}\right) + 64I_{ref}\left(1 + 0.125\frac{I_x}{I_{ref}}\right)^4 \tag{A.1}$$

$$I_{num} == 64I_{ref}\left[0.025 + \frac{\Delta I_{ref}}{64I_{ref}} + \left(1 + 0.125\frac{I_x}{I_{ref}}\right)^4\right] \tag{A.2}$$

$$I_{den} = \left(1.6I_{ref} + \Delta I_{ref}\right) + 64I_{ref}\left(1 - 0.125\frac{I_x}{I_{ref}}\right)^4 \tag{A.3}$$

$$I_{den} = 64I_{ref}\left[0.025 + \frac{\Delta I_{ref}}{64I_{ref}} + \left(1 - 0.125\frac{I_x}{I_{ref}}\right)^4\right] \tag{A.4}$$

By recall equation (2.55), the output current of the proposed EXPFG will be

$$I_{out} = I_w\frac{I_{num}}{I_{den}} = I_w\left\{\frac{\left[k+\left(1+0.125\frac{I_x}{I_{ref}}\right)^4\right]}{\left[k+\left(1-0.125\frac{I_x}{I_{ref}}\right)^4\right]}\right\} \tag{A.5}$$

where $k = 0.025 + \frac{\Delta I_{ref}}{64I_{ref}}$. Assume that there is ±10% deviation from the exact value (0.025); the results show that the deviation is not significant.

Chapter 4:

Referring to chapter (4) section (4.2) and section (4.3), if $I_{bias} = 2I_{ref} + \Delta I$ then:

$\propto = \frac{2I_{ref}+\Delta I}{2I_{ref}} = 1 + \frac{\Delta I}{2I_{ref}}$

$\propto = 1 + \Delta\propto$

where $\Delta\propto = \frac{\Delta I}{2I_{ref}}$ is a very small value represents the error amount.

then equation (4.3) can be rewritten as follows:

$$I_{node3} = I_w \left(\frac{I_{in1}I_{in2}}{I_{x1}I_{x2}}\right)\left(\frac{I_{in1}I_{in2}}{I_{x1}I_{x2}}\right)^{\Delta\propto} \tag{A.6}$$

equations (4.10) and (4.11) can expressed as

$$I_{node3} = I_w \left[\frac{I_{y1}I_{y2}+I_{y1}i_{y2}+I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right]\left[\frac{I_{y1}I_{y2}+I_{y1}i_{y2}+I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right]^{\Delta\propto} \tag{A.7}$$

$$I_{node4} = I_w \left[\frac{I_{y1}I_{y2}-I_{y1}i_{y2}-I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right]\left[\frac{I_{y1}I_{y2}-I_{y1}i_{y2}-I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right]^{\Delta\propto} \tag{A.8}$$

Assume that $\delta_1 = \left[\frac{I_{y1}I_{y2}+I_{y1}i_{y2}+I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right]^{\Delta\propto}$ and $\delta_2 = \left[\frac{I_{y1}I_{y2}-I_{y1}i_{y2}-I_{y2}i_{y1}+i_{y1}i_{y2}}{I_{x1}I_{x2}}\right]^{\Delta\propto}$

$$I_{node5} = I_w \left\{\frac{(I_{y1}I_{y2}+I_{y1}i_{y2}+I_{y2}i_{y1}+i_{y1}i_{y2})\delta_1+(I_{y1}I_{y2}-I_{y1}i_{y2}-I_{y2}i_{y1}+i_{y1}i_{y2})\delta_2}{I_{x1}I_{x2}}\right\} \tag{A.9}$$

$$I_{node5} = I_w \left\{\frac{I_{y1}I_{y2}(\delta_1+\delta_2)+I_{y1}i_{y2}\delta_1-I_{y1}i_{y2}\delta_2+I_{y2}i_{y1}\delta_1-I_{y2}i_{y1}\delta_2+i_{y1}i_{y2}(\delta_1+\delta_2)}{I_{x1}I_{x2}}\right\} \tag{A.10}$$

$$I_{node5} = I_w \left\{\frac{(I_{y1}I_{y2}+i_{y1}i_{y2})(\delta_1+\delta_2)}{I_{x1}I_{x2}} + \frac{(I_{y1}i_{y2}+I_{y2}i_{y1})\delta_1-(I_{y1}i_{y2}+I_{y2}i_{y1})\delta_2}{I_{x1}I_{x2}}\right\} \tag{A.11}$$

With $\delta_1 + \delta_2 = 2 + \Delta\delta$

$$I_{node5} = I_w \left\{\frac{2(I_{y1}I_{y2}+i_{y1}i_{y2})}{I_{x1}I_{x2}} + \Delta\delta\frac{(I_{y1}I_{y2}+i_{y1}i_{y2})}{I_{x1}I_{x2}} + (\delta_1-\delta_2)\frac{(I_{y1}i_{y2}+I_{y2}i_{y1})}{I_{x1}I_{x2}}\right\} \tag{A.12}$$

$$I_{node5} = \frac{2I_w i_{y1}i_{y2}}{I_{x1}I_{x2}} + \frac{2I_w I_{y1}I_{y2}}{I_{x1}I_{x2}} + \Delta\delta\frac{I_w(I_{y1}I_{y2}+i_{y1}i_{y2})}{I_{x1}I_{x2}} + (\delta_1-\delta_2)\frac{I_w(I_{y1}i_{y2}+I_{y2}i_{y1})}{I_{x1}I_{x2}} \tag{A.13}$$

Moreover, if k is not exact (i.e. $k = \frac{2I_w I_{y1}I_{y2}}{I_{x1}I_{x2}} + \Delta k$), equation (4.13) can be modified to read

$$I_{out} = \frac{2I_w i_{y1}i_{y2}}{I_{x1}I_{x2}} + \Delta k + \Delta\delta\frac{I_w(I_{y1}I_{y2}+i_{y1}i_{y2})}{I_{x1}I_{x2}} + (\delta_1-\delta_2)\frac{I_w(I_{y1}i_{y2}+I_{y2}i_{y1})}{I_{x1}I_{x2}} \tag{A.14}$$

Appendix B

Publications

During this study, the following journal and conference papers were produced:

Patents/ Disclosures:

[1] Karama M. AL-Tamimi and Munir A. AL-Absi "*A Controllable Current-Mode CMOS Logarithmic Function Circuit*," filed with the U.S. Patent and Trademark Office (USPTO), U.S.A, on March 12, 2012, Docket# 33000.61.

Refereed Journal /Magazine Articles:

[1] Munir Al-Absi and Karama Al-Tamimi, " A CMOS Current-Mode Log(x) and Log(1/x) Functions Generator", under review in International Journal of Electronics (IJE)

[2] Munir Al-Absi and Karama Al-Tamimi, " Logarithmic-Control Variable Gain Amplifier (LCVGA), submitted to International Journal of Electronics

[3] Karama Al-Tamimi & Munir Al-Absi, "Taylor Series-Based Current Mode CMOS logarithmic Circuit, Submitted to AEU - International Journal of Electronics and Communications

[4] Karama AL-Tamimi and Munir AL-Absi "Realization of 96 dB-Linear Exponential Current Generator" To be submit to Analog Integrated Circuits and Signal Processing, Springer.

Refereed Conference Publications:

[1] Karama AL-Tamimi and Munir A. AL-Absi, "A new CMOS Current-Mode Logarithmic Circuit," IEEE Student Conference on Research and Development, 2012, pp 82-86

[2] Karama AL-Tamimi and Munir A. AL-Absi , "A Novel Logarithmic Current-Controlled Current Amplifier (LCCA)", World Academy of Science, Engineering and Technology , Vol. 61, 2012, pp. 496-498

[3] Munir A. AL-Absi and Karama AL-Tamimi, "A Current-Mode Controllable Logarithmic Function Circuit using MOSFET in Subthreshold" , Proceedings of The World Congress on Engineering and Computer Science (WCECS 2012) 2012, pp844-846

[4] Karama AL-Tamimi and Munir A. AL-Absi, "An Ultra Low Power High Accuracy Current-Mode CMOS Squaring Circuit " , Proceedings of The World Congress on Engineering and Computer Science 2012, pp872-874

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